GRF2501

Preliminary **High Gain, Ultra-Low Noise Amplifier**
802.11 a/n/ac 4.9 - 6.0 GHz

Package: 6-Pin DFN

Features

- 4.9 GHz to 6 GHz Operation
- 0.75 dB Noise Figure
- 16.5 dB Flat Gain
- 2.7 V to 5.0 V Single Supply
- Internally Matched to 50 Ω
- High Directivity
- Unconditionally Stable

Applications

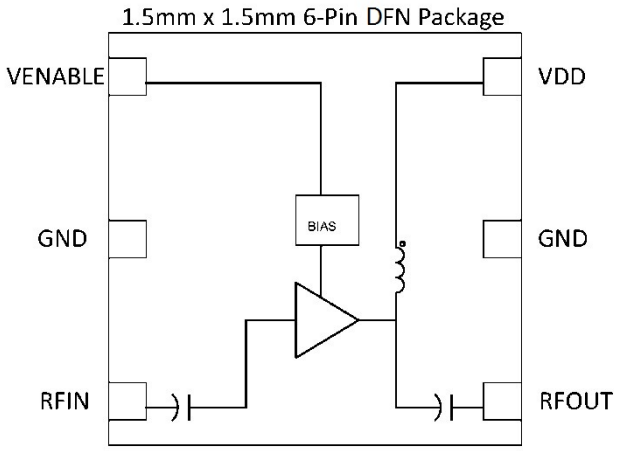
- WiFi Access Points
- Mobile WiFi Devices
- Microwave Backhaul
- 802.11p Vehicle Communications

Product Description

The GRF2501 is an ultra-low noise amplifier (LNA) designed for IEEE 802.11a/n/ac/p applications (5.1 GHz to 5.925 GHz). Over this band, the device exhibits outstanding noise figure (NF) of 0.75 dB along with excellent gain flatness and high linearity. The high gain, superior NF and directivity of its design allows designers to create receiver architectures with outstanding cascaded NF and unconditional stability.

The LNA is operated from a single positive supply of 2.7 V to 5.0 V with a typical bias condition of 3.3 V and 13 mA. GRF2501 is housed in a 1.5 x 1.5 x 0.5 mm 6-pin plastic DFN package and is internally matched to 50 Ω at the input and output ports.

Functional Block Diagram



Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	0	6.0	V
DC Voltage at Control Port (Pin 1)	V_{ENABLE}	0	5.0	V
RF CW Power into LNA Input	$P_{IN\ MAX}$		+15	dBm
Operating Temperature (package heat sink)	T_{AMB}	-40	+105	°C
Storage Temperature	T_{STG}	-40	+150	°C
Maximum Channel Temperature	T_{MAX}		+160	°C
Maximum Disspated Power	$P_{DISS\ MAX}$		200	mW
Electro Static Discharge:				
Charged Device Model: (TBD)	CDM	Class 4: 1000		V
Human Body Model: (TBD)	HBM	Class 1B: 500		V
Machine Model: (TBD)	MM	Class A: 50		V

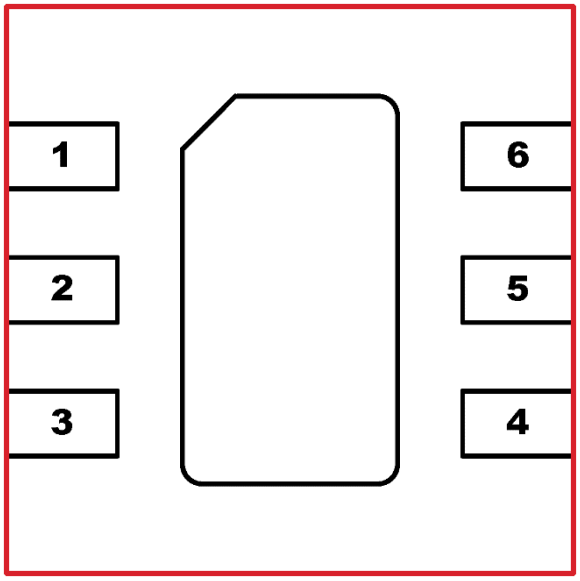
Caution! ESD Sensitive Device

Exceeding Absolute Maximum Rating conditions may cause permanent damage to the device.

Nominal Operating Parameters

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
High Gain Mode						V_{DD} = 3.3 V, V_{ENABLE} = 3.3 V, T_A = 25°C
Test Frequency	F_{TEST}		5500		MHz	
Gain	S21	15.0	16.5		dB	
Gain Flatness	ΔS21		+/- 0.5		dB	Across 5.1 to 5.825 GHz
Input Return Loss	S11		-19		dB	
Output Return Loss	S22		-17		dB	
Noise Figure	NF		0.75		dB	(Board Losses De-embedded)
Input 3rd Order Intercept	IIP3		+9.0		dBm	
Input 1dB Compression	IP1dB	-9.5	-8.0		dBm	In band
Input 1dB Compression (2450 MHz)	IP1dB		-9.0		dBm	Out of band
Supply Current (Quiescent)	I_{DDQ}	10.5	13	15.5	mA	
Enable Current	I_{ENABLE}		270	500	uA	Ienable is roughly 2% of Iddq
Disabled Mode						V_{DD} = 3.3 V, V_{ENABLE} = 0V
Supply Current (Leakage)	I_{DD}		47	100	µA	
Enable Current	I_{ENABLE}		0.01	2	µA	
Thermal Data						
Thermal Resistance (Infra-Red Scan)	Θjc		141		°C/W	
Channel Temperature @ +85 C reference (Package heat sink)	$T_{CHANNEL}$		+91		°C	Vdd: 3.3 V; Iddq: 12 mA; No RF; Dissipated Power: 40 mW

Pin Out (Top View)

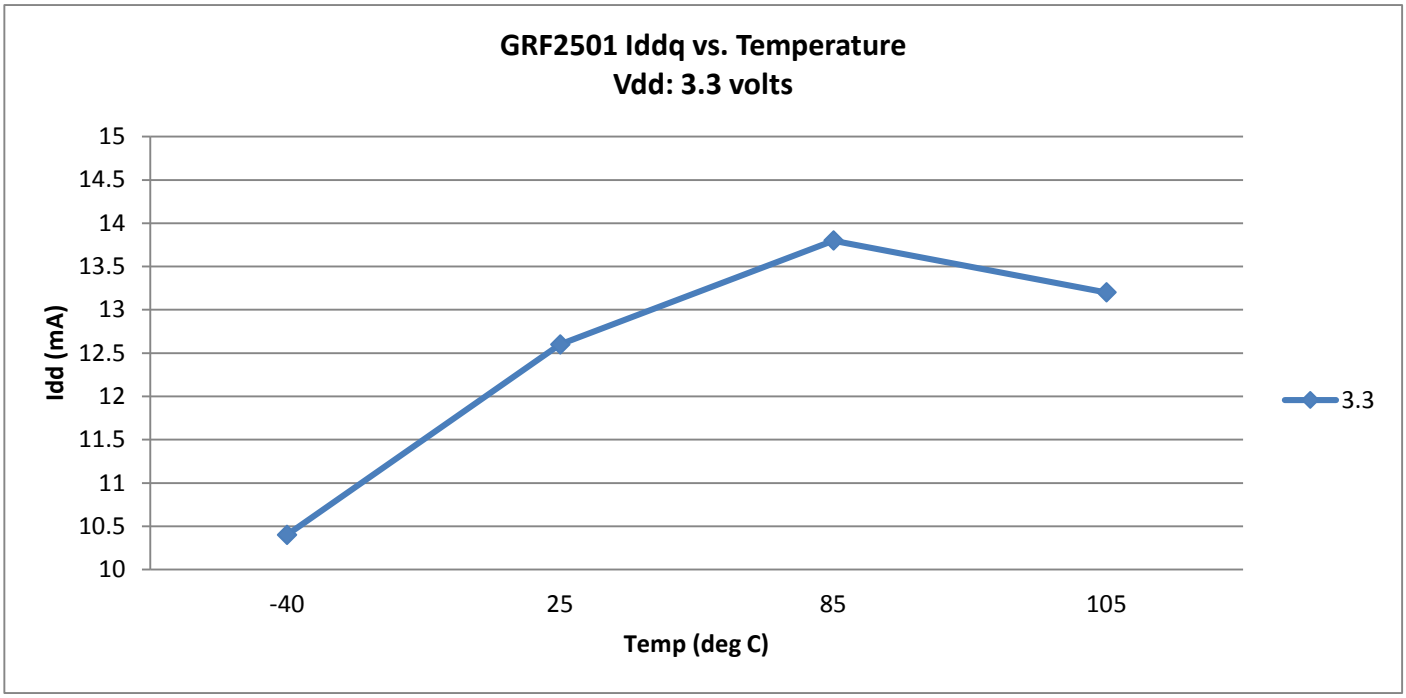


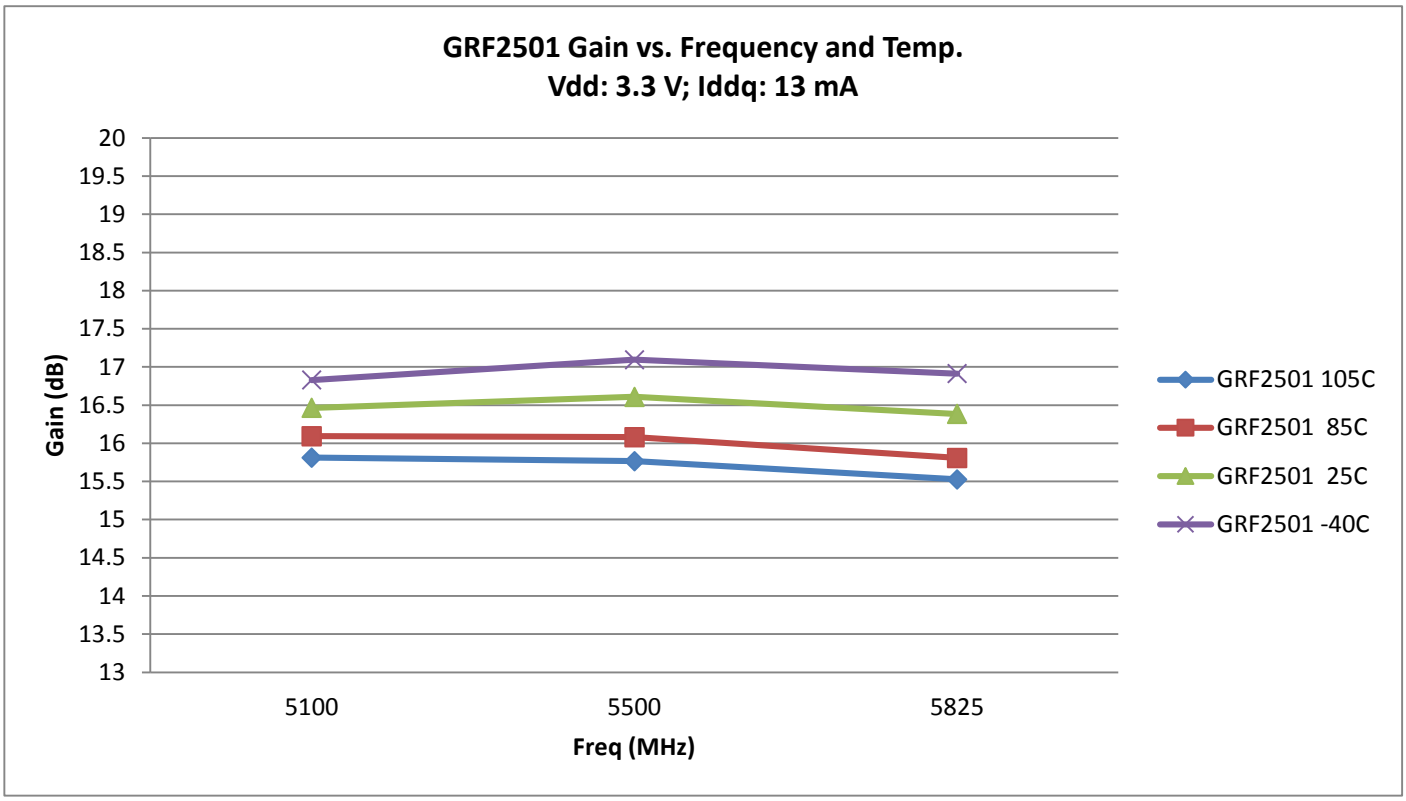
Pin Assignments

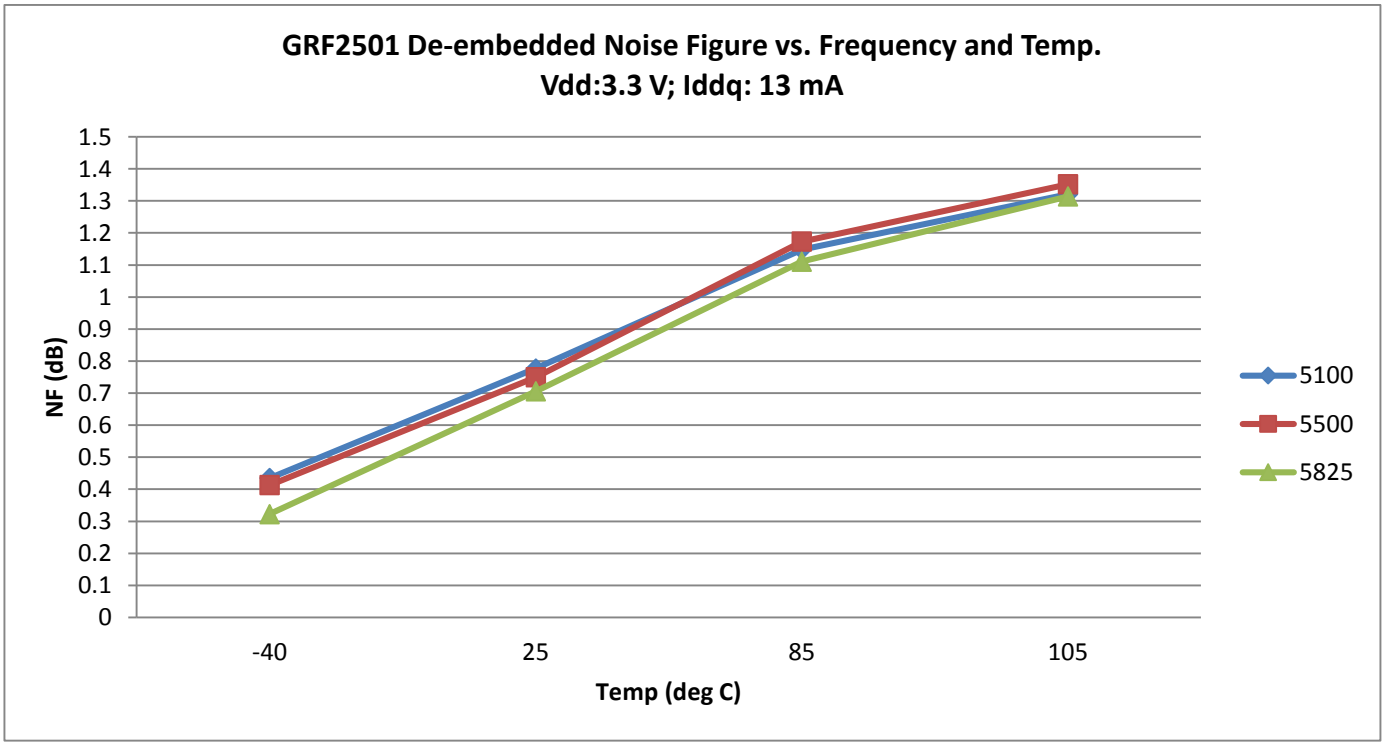
Pin	Name	Description	Note
1	VENABLE	LNA Enable	Increase voltage to draw more current and increase IP3.
2	GND	Ground	Connect to ground for maximum RF performance
3	RFIN	LNA RF input	Internally matched to 50 Ω. These ports may be DC connected to ground externally but no DC > 0.2 volts should be applied to these ports.
4	RFOUT	LNA RF output	
5	GND	Ground	Connect to ground for maximum RF performance
6	VDD	Supply Voltage for the LNA	Requires bypass capacitance as close as possible to pin on PCB
PKG BASE	GND	Ground	Provides DC and RF ground for LNA, as well as thermal heat sink. Please see evaluation board assembly diagram for reference.

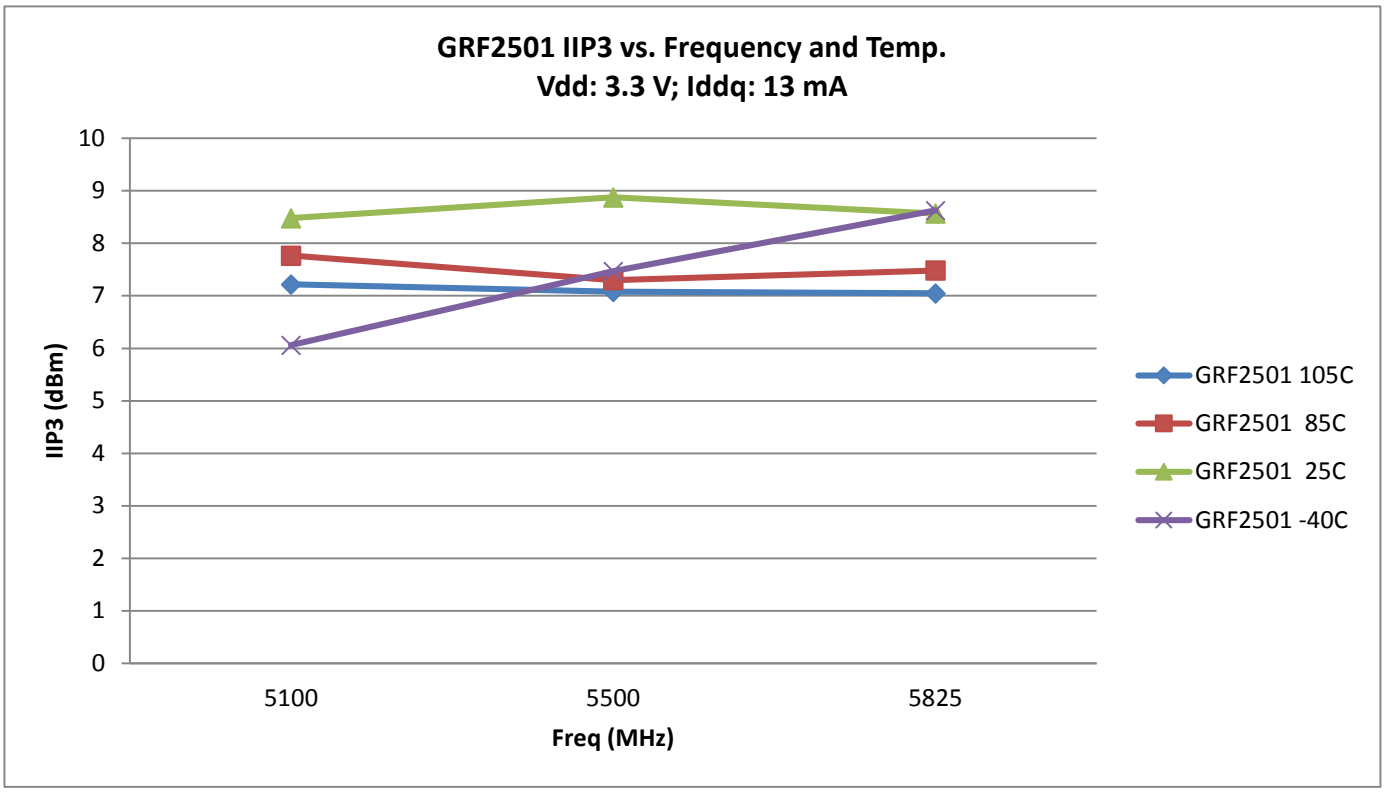
V_{ENABLE} Truth Table

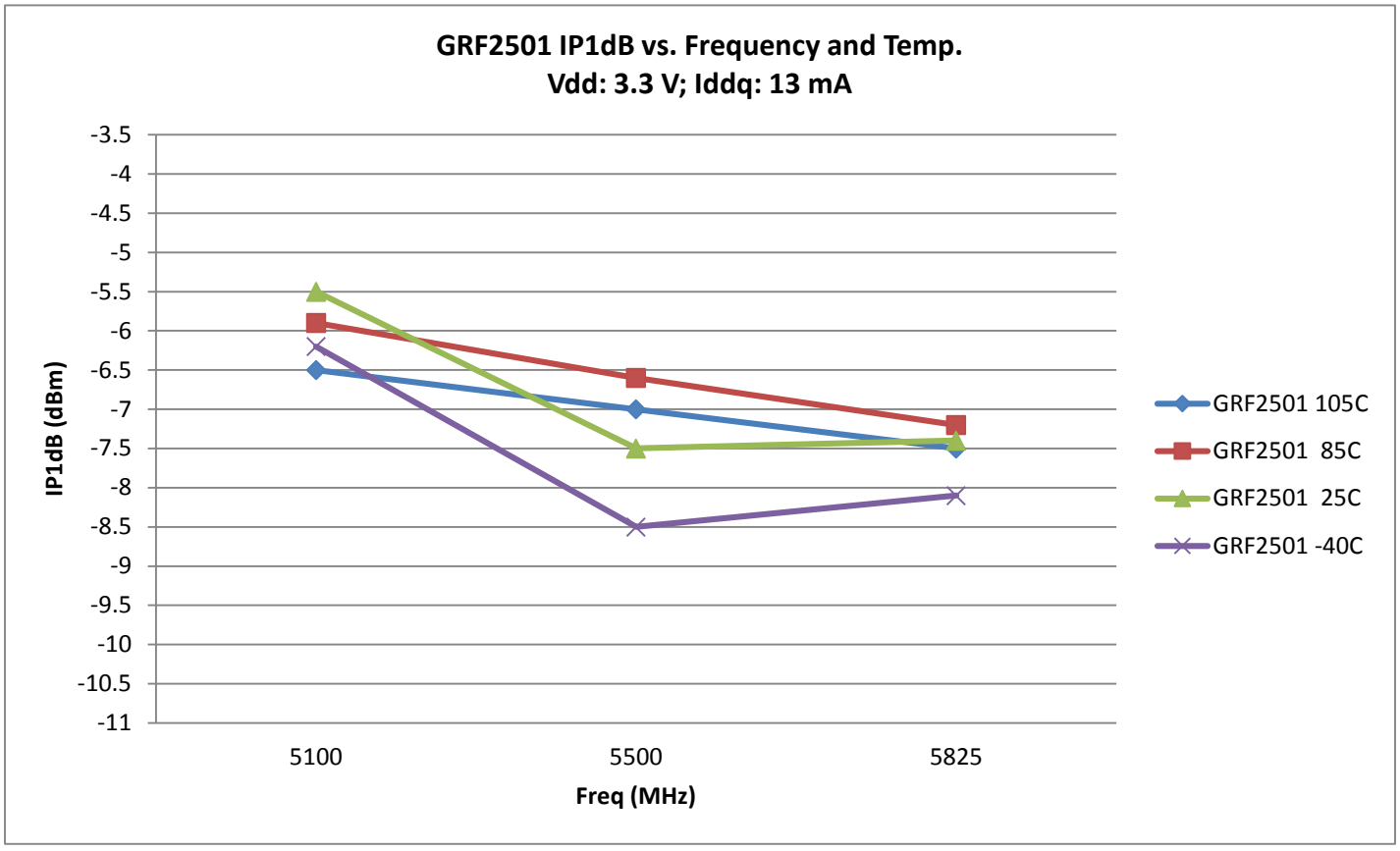
V_{ENABLE}	Mode
>=1.8 V	LNA On
<0.5 V	LNA Off

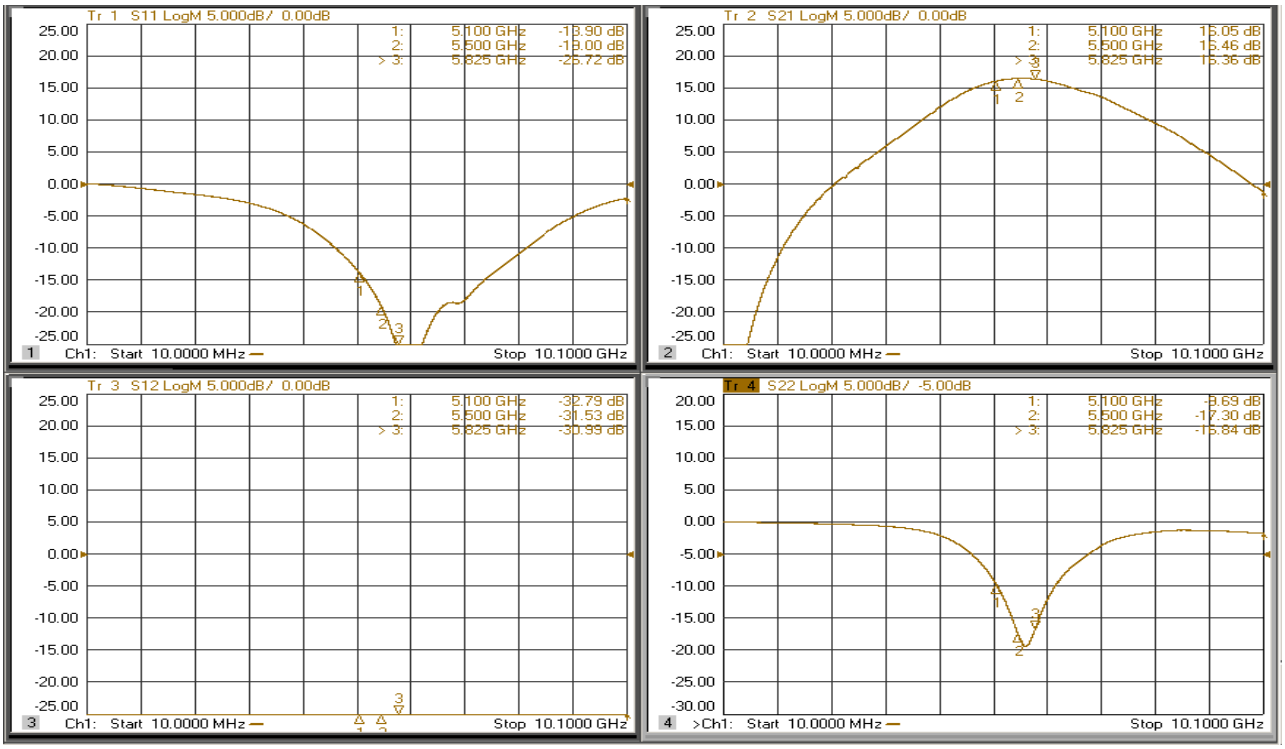

GRF2501 Iddq vs. Temperature
Vdd: 3.3 volts
Idd (mA)
15
14.5
14
13.5
13
12.5
12
11.5
11
10.5
10
-40
25
85
105
Temp (deg C)
3.3


GRF2501 Gain vs. Frequency and Temp.
Vdd: 3.3 V; Iddq: 13 mA
Gain (dB)
20
19.5
19
18.5
18
17.5
17
16.5
16
15.5
15
14.5
14
13.5
13
5100
5500
5825
Freq (MHz)
GRF2501 105C
GRF2501 85C
GRF2501 25C
GRF2501 -40C

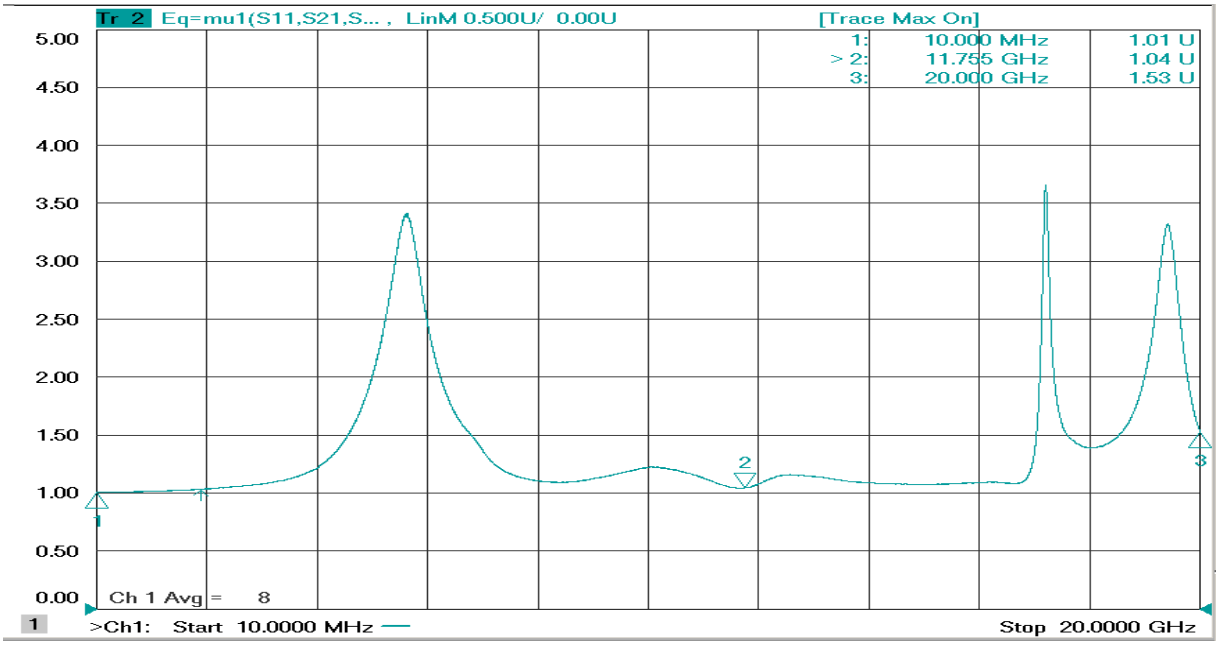

GRF2501 De-embedded Noise Figure vs. Frequency and Temp.
Vdd:3.3 V; Iddq: 13 mA
NF (dB)
1.5
1.4
1.3
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-40
25
85
105
Temp (deg C)
5100
5500
5825


GRF2501 IIP3 vs. Frequency and Temp.
Vdd: 3.3 V; Iddq: 13 mA
IIP3 (dBm)
10
9
8
7
6
5
4
3
2
1
0
5100
5500
5825
Freq (MHz)
GRF2501 105C
GRF2501 85C
GRF2501 25C
GRF2501 -40C


GRF2501 IP1dB vs. Frequency and Temp.
Vdd: 3.3 V; Iddq: 13 mA
IP1dB (dBm)
-3.5
-4
-4.5
-5
-5.5
-6
-6.5
-7
-7.5
-8
-8.5
-9
-9.5
-10
-10.5
-11
5100
5500
5825
Freq (MHz)
GRF2501 105C
GRF2501 85C
GRF2501 25C
GRF2501 -40C



GRF2501 Evaluation Board S-parameters



GRF2501 Evaluation Board Stability Mu Factor

GRF2501 Theory of Operation:

The GRF2501 is matched on-die to offer good return losses, flat gain and outstanding linearity over 4.9 – 6.0 GHz. Implementation of this device requires few external components as follows:

M1: This resistor is used in series with Venable to set the device Iddq. The die is designed to draw a typical 13 mA with 3.3 V applied directly to pin 1 of the device thus M1 is not necessary under this bias condition. For higher Venable levels such as 5 volts, M1 can be used to adjust Iddq downward as desired. On the evaluation board, this component uses a 0402 package but a smaller size can be used if desired since Ienable is small.

M2: DNP

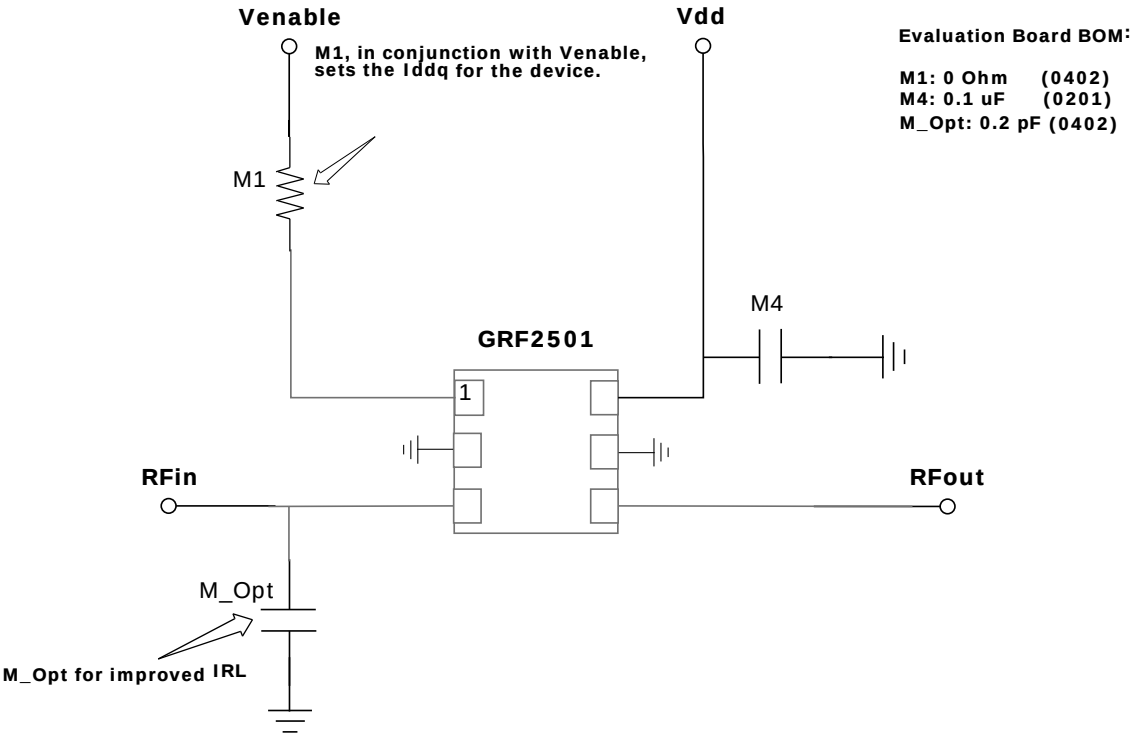
M3: DNP

M4: Bias de-coupling capacitor that should be placed as close as possible to pin 6 of the device. A small package size is recommended here so as to place M4 as close as possible to pin 6.

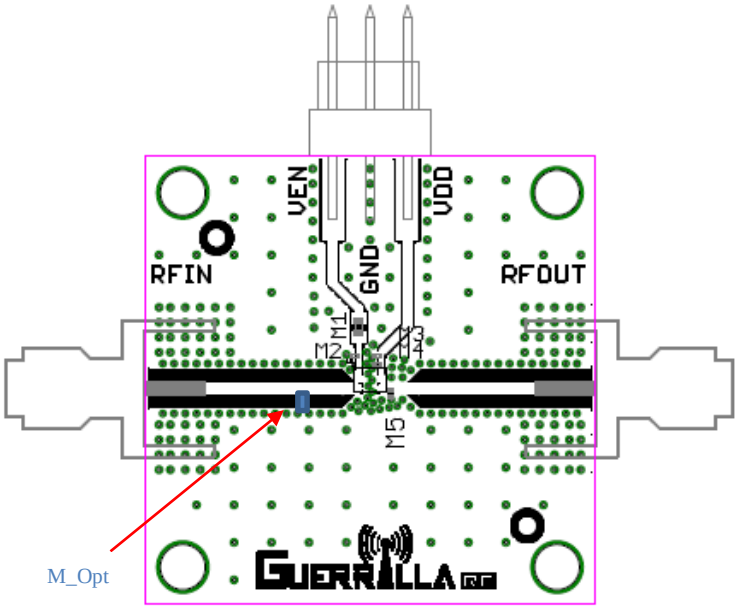
M5: This is currently a 20k Ohm resistor used as part of the DC bias network but it should still be placed close to the device package to assure a compact layout. Package size is not critical.

M_Opt: This is an additional 0.2 pF cap to ground added to optimize the device input return loss and gain. It also serves to slightly improve the device NF. Due to layout constraints on the evaluation board, a 0402 package size was chosen for this component. In a customer layout, this component can easily be in a smaller package if desired.

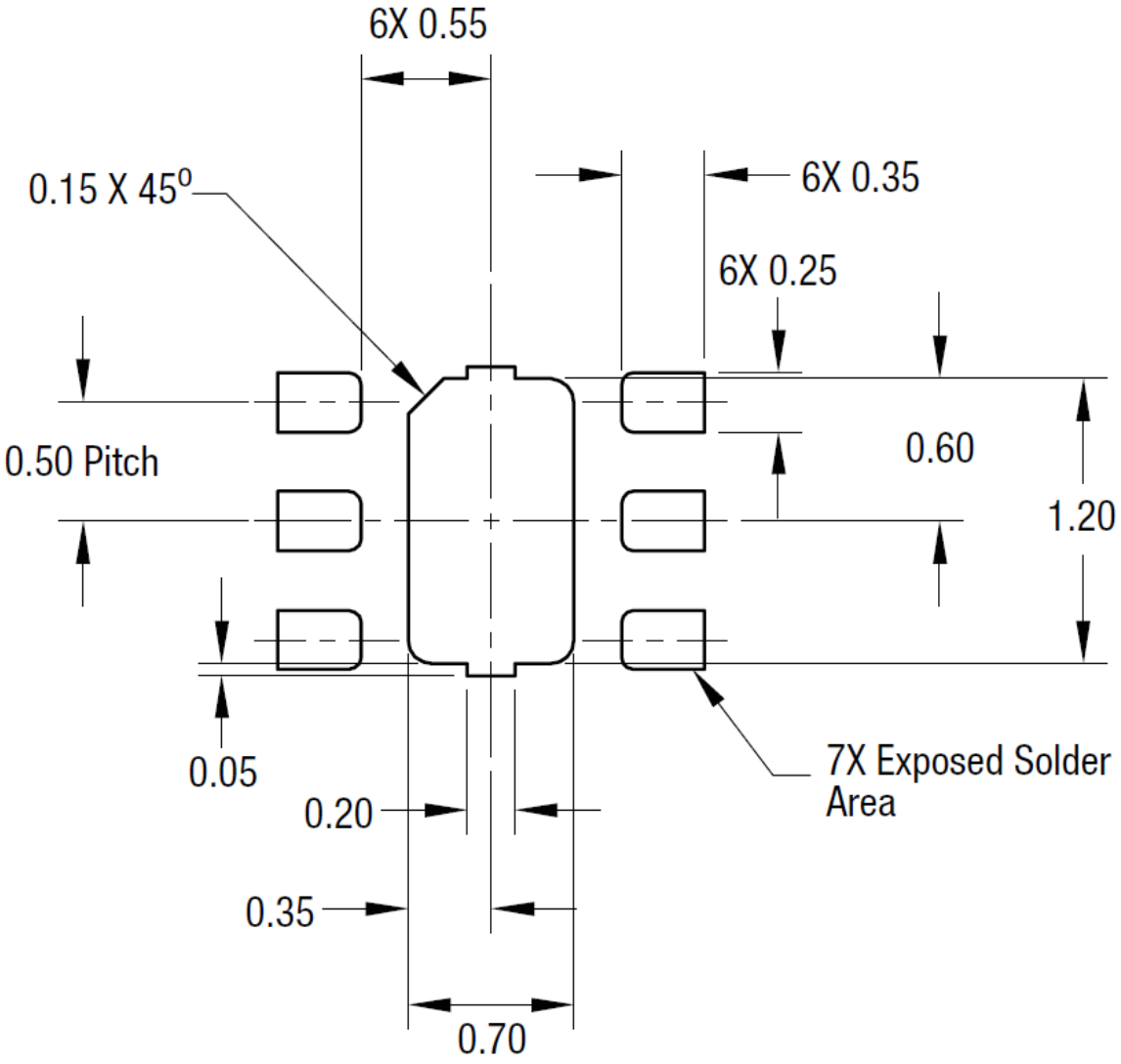
Regarding Matching: The device is internally matched but having an additional set of pads for a potential shunt matching element on both the device input and output is a good idea so that the device can be fully optimized within a particular layout. In that way, the extra pads can be used or not used as required. Also, the device has internal DC blocks on the RF input/output so there is no DC on pins 3 and 4. However, DC voltages greater than 0.2 V should not be applied to these pins externally.



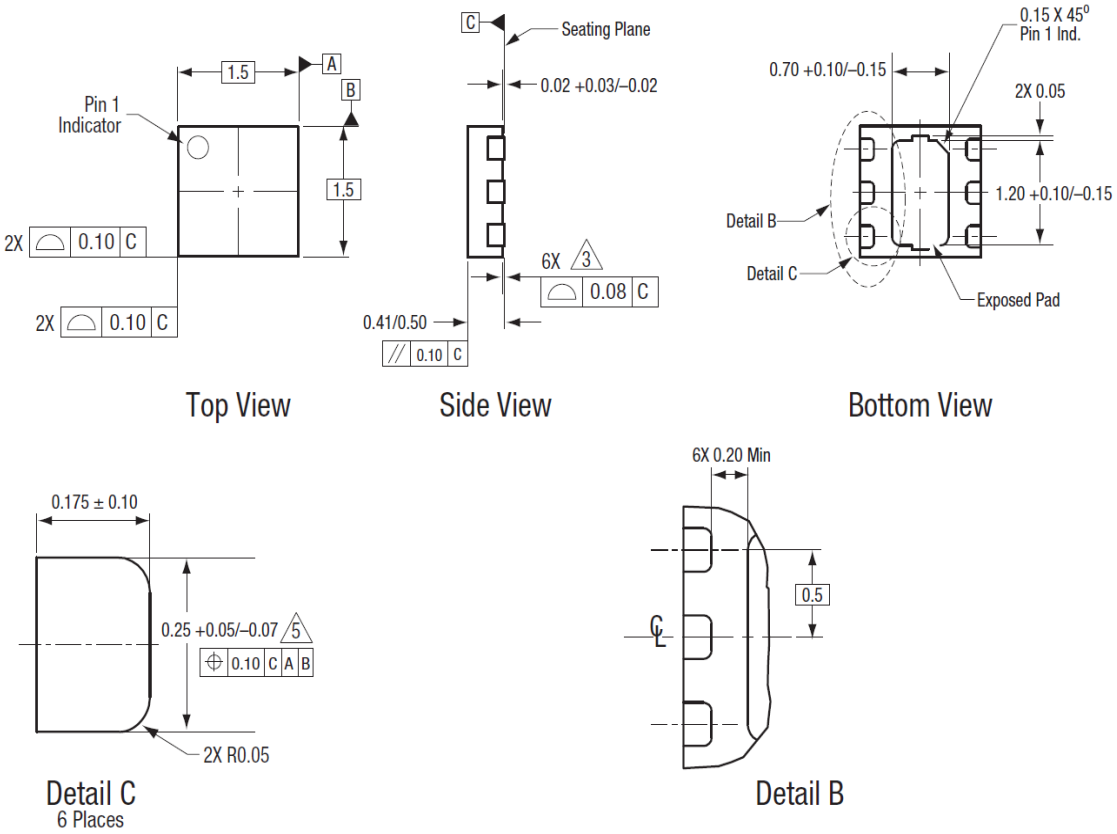
GRF2501 Evaluation Board Application Schematic



GRF2501 Evaluation Board Assembly Diagram



GRF2501 1.5mm x 1.5mm 6-Pin DFN PCB Layout Footprint



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed heat sink slug as well as the terminals..
Plating requirement per source control drawing (SCD) 2504.
Dimension applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

GRF2501 6-Pin DFN Package Dimensions

Data Sheet Release Status:	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry supplied transistor s-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on evaluation board measurements in the Guerrilla RF Applications Lab.
Released	All data based on device qualification data. Typically, this data is nearly identical to the data found in the preliminary version. Max and min values for key RF parameters are included.