High Frequency, Low Jitter VCXO

CONNOR WINFIELD

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Description

The Connor-Winfield models V777, V778, V787 and V788 are 3.3V, Surface Mount 5.0x7.0mm, Voltage Controlled Crystal Oscillator (VCXO) with LVPECL differential outputs and enable/disable function. The V777, V778, V787 and V788 are designed for use with applications utilizing a PLL system requiring very high frequency and low jitter. The surface mount package is designed for high-density mounting and is optimum for mass production.

Features

- 3.3V Operation
- Absolute Pull Range (APR): ±30ppm
- Temperature Range: 0 to 70°C or -40 to 85°C
- Differencial LVPECL Outputs
- Low Jitter 70fs RMS Typical
- Enable / Disable Function:
  - Models: V777-V787: Enable Low
  - Models: V778-V788: Enable High
- 5.0x7.0mm Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Lead Free ✓RoHS

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.5	-	4.6	Vdc	
Input Voltage (Vc)	-0.5	-	Vcc+0.5	Vdc	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Center Frequency: (Fo)	150	-	710	MHz	
Operating Temperature Range:					
Models: V777-V778	0	-	70	°C	
Models: V787-V788	-40	-	85	°C	
Supply Voltage: (Vcc)	3.135	3.30	3.465	Vdc	
Supply Current (Icc)	-	-	100	mA	
Integrated Phase Jitter (BW=12kHz to 20MHz)	-	70	100	fs RMS	
Typical Phase Noise for Fo = 245.76 MHz					
SSB Phase Noise at 10Hz offset	-	-60	-	dBc/Hz	
SSB Phase Noise at 100Hz offset	-	-85	-	dBc/Hz	
SSB Phase Noise at 1KHz offset	-	-110	-	dBc/Hz	
SSB Phase Noise at 10KHz offset	-	-135	-	dBc/Hz	
SSB Phase Noise at 100KHz offset	-	-150	-	dBc/Hz	
SSB Phase Noise at 1MHz offset	-	-150	-	dBc/Hz	
SSB Phase Noise at 10MHz offset	-	-158	-	dBc/Hz	
Sub Harmonic Content					
@ 25% Fo	-	-45	-	dBc	
@ 50% Fo		-40	-	dBc	
@ 75% Fo		-45	-	dBc	
Harmonic Content @ 2xFo	-	-17	-	dBc	
Spurious Content	-	-	-70	dBc	2

Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Control Voltage Range (Vc)	0.3	1.65	3.0	Vdc	
Tuning Slope (Kv)	-	80	-	ppm/V	
Absolute Pull Range: (APR)	±30	-	-	ppm	1
Monotonic Linearity	-10	-	10	%	
Input Impedance	130K	180K	-	Ohm	
Modulation Bandwidth (3dB)	25	-	-	KHz	
Models: V777-V787 Enable / Disable Function					
Enable Input Voltage (Low) (Vil)	-	-	1.68	Vdc	
Disable Input Voltage (High) (Vih)	2.275	-	-	Vdc	2
Models: V778-V788 Enable / Disable Function					
Enable Input Voltage (High) (Vil)	2.275	-	-	Vdc	
Disable Input Voltage (Low) (Vih)	-	-	1.68	Vdc	2

LVPECL Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load -	-	-	50	Ohms	3
Voltage (High) Voh	2.275	-	-	Vdc	
(Low) Vol	-	-	1.68	Vdc	
Duty Cycle at 50% Level	45	50	55	%	
Rise / Fall Time 20% to 80%	-	0.30	0.45	ns	

RoHS COMPLIANT

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Packaging Characteristics

Package	Hermetically sealed ceramic package with grounded metal cove
Soldering Process	RoHS compliant, lead free. See Solder Profile

Notes

1. *Absolute pull range (APR) is the minimum guaranteed pull range of the VCXO under all conditions over the lifetime operation. Including calibration @ 25°C, frequency vs change in temperature, frequency vs. change in supply voltage, frequency vs. change in load, shock and vibration and aging for ten years. The APR is referenced to Fo. Positive Transfer Function*
2. *Outputs are enabled with no connection on pad 2. When oscillator is disabled both outputs are in high impedance state.*
3. *50 ohm termination into Vcc-2V or Thevein equivalent*

Enable / Disable Function

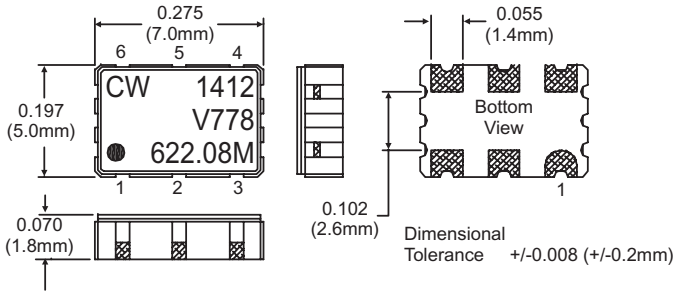
Models: V777-V787

Enable / Disable Function (Pad 2)	Output
No Connection	Enable
Low	Enable
High	Disable (High Impedance)

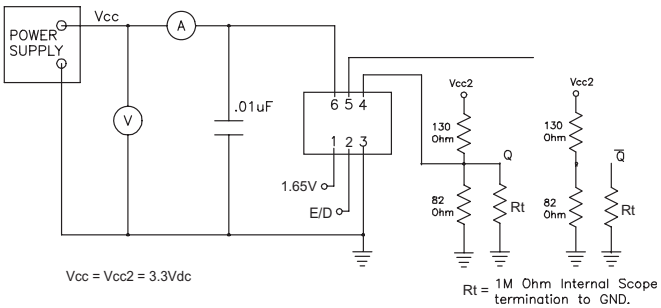
Models: V778-V788

Enable / Disable Function (Pad 2)	Output
No Connection	Enable
High	Enable
Low	Disable (High Impedance)

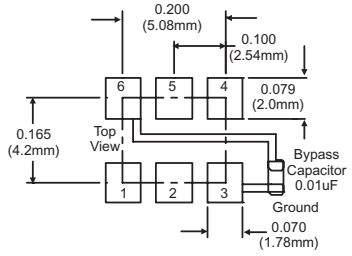
Package Layout



Test Circuit



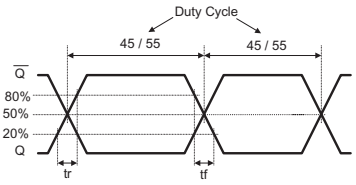
Suggested Pad Layout



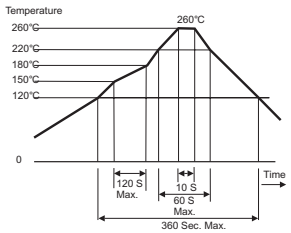
Pad Connections

Pad	Pad Connection
1	Control Voltage
2	Enable / Disable
3	Ground (Case)
4	Output Q
5	Output $\overline{Q}$
6	Vcc

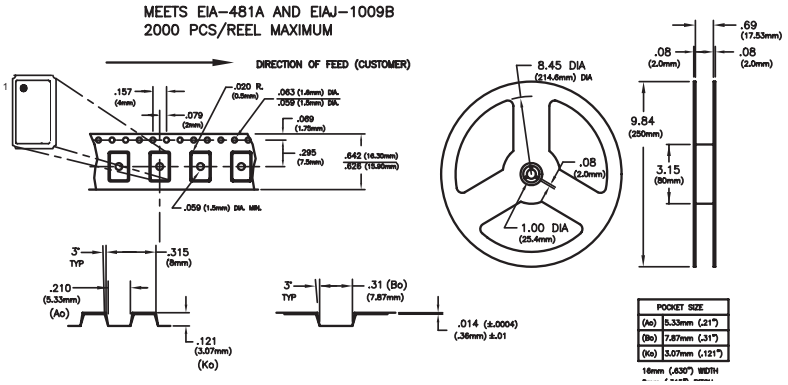
Output Waveform



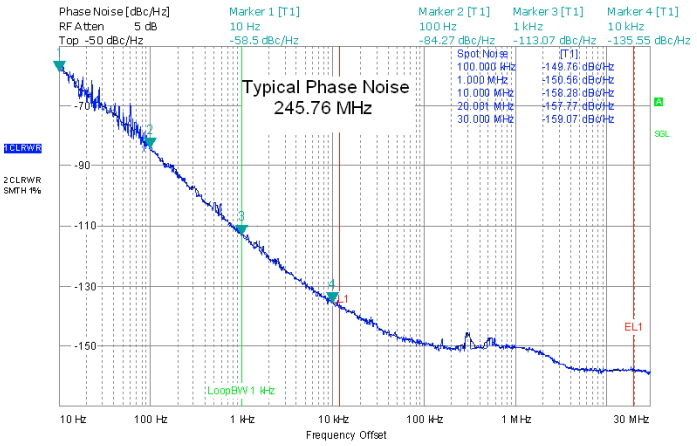
Solder Profile



Tape and Reel



Phase Noise Plot



Ordering Information

V 7	7	8	-	622.08M
___	Temperature Range: 7 = 0 to 70° C 8 = -40 to 85° C APR: +/-30ppm	Enable/Diasble: 7= Enable Low 8 = Enable High Supply Voltage: 3.3Vdc		Output Frequency: Frequency Format -xxx.xM Min.* -xxx.xxxxxxM Max.* *Amount of numbers after the decimal point. M = MHz

Example:
V778-622.08M = 5x7mm, LVPECL, VCXO
3.3Vdc, -40 to 85°C, ±30APR,
Output Frequency 622.08MHz

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Revision	04
Date	06 June 2014

Specifications subject to change without notification. See Connor-Winfield's website for latest revision. All dimensions in inches.
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