Product Specification

PE42650A

SP3T High Power UltraCMOS™
RF Switch 30 MHz - 1000 MHz

Features

- 50 Watt P1dB compression point
- 10 Watts <8:1 VSWR (Normal Operation)
- 38 dB TX-RX Isolation
- $2f_o$ and $3f_o$ < -81 dBc @10 Watts
- ESD rugged to 2.0 kV HBM
- No blocking capacitors required
- 32-lead 5x5 mm QFN package

Product Description

The following specification defines an SP3T (single pole three throw) switch for use in cellular and other wireless applications. It has both a standard and attenuated RX mode. The PE42650A uses Peregrine's UltraCMOS™ process and also features HaRP™ technology enhancements to deliver high linearity and exceptional harmonics performance. HaRP™ technology is an innovative feature of the UltraCMOS™ process providing upgraded linearity performance.

The PE42650A is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

End of Life

Figure 1. Functional Diagram

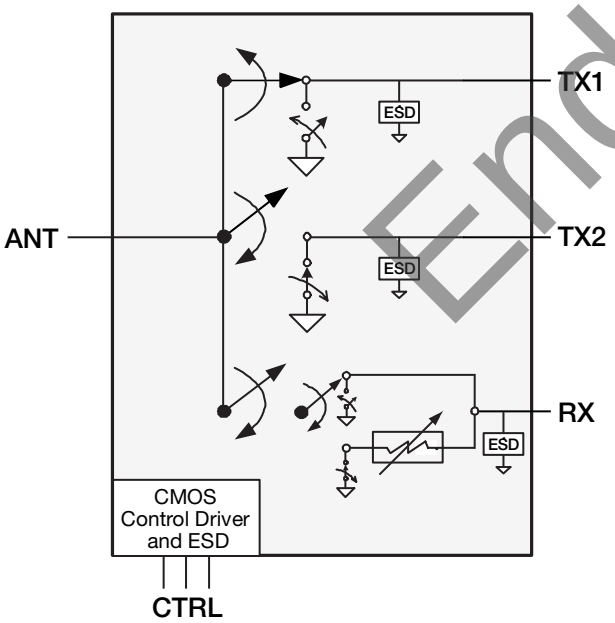
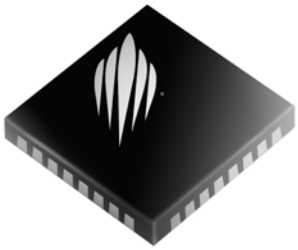


Figure 2. Package Type
32-lead 5x5 mm QFN



©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Table 1: Electrical Specifications @ +25 °C, V_{DD} = 3.3 V (Z_S = Z_L = 50 Ω) unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
TX Insertion Loss[1]	30 MHz ≤ 1 GHz		0.3	0.5	dB
RX Insertion Loss (Un-Attenuated State)[1]	30 MHz ≤ 1 GHz		0.5	0.9	dB
RX Insertion Loss (Attenuated State)[1]	800 MHz	13	14.5	16	dB
0.1 dB Input Compression Point	800 MHz, 50% duty cycle		45.4		dBm
Isolation (Supply Biased): TX-TX	800 MHz	30	33		dB
Isolation (Supply Biased): TX-RX	800 MHz	35	38		dB
Unbiased Isolation: ANT - TX, V_{DD}, V1, V2, V3=0 V	800 MHz, +27 dBm	6	10		dB
Unbiased Isolation: ANT - RX, V_{DD}, V1, V2, V3=0 V	800 MHz, +27 dBm	14	22		dB
RX Port Return Loss[1]	Un-Attenuated State, 800 MHz	18	22		dB
	Attenuated State, with external matching inductor optimized without attenuator engaged, 800 MHz	12	18		dB
TX and ANT Port Return Loss[1]	800 MHz	20	23		dB
TX, 2nd Harmonic TX, 3rd Harmonic	800 MHz @ 42.5 dBm 800 MHz @ 42.5 dBm		-81 -81	-79 -79	dBc dBc
RX IIP3	Un-Attenuated State, 800 MHz, 150 kHz tone separation	30			dBm
Switching Time	50% of CTRL to 10/90% of RF		0.1	0.5	ms

Note: 1. The device was matched with ~4 nH inductance per RF port. RX port may not need matching inductor.

Table 2. Operating Ranges

Parameter	Min	Typ	Max	Units
Frequency Range	30		1000	MHz
TX Input Power[1] (VSWR ≤ 8:1)			40	dBm
RX Input Power[2] (VSWR ≤ 8:1)			27	dBm
V_{DD} Power Supply Voltage	3.2	3.3	3.4	V
I_{DD} Power Supply Current		90	170	uA
Control Voltage High	1.4			V
Control Voltage Low			0.4	V
T_{OP} Operating temperature range (Case)	-40		85	°C
T_j Operating junction temperature			140	°C

Notes: 1. Supply biased
2. Supply biased or unbiased

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42650A in the 5x5 QFN package is MSL3.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{CASE}	Maximum case temperature		85	°C
T_j	Peak maximum junction temperature (10 seconds max)		200	°C
P_{IN}	TX Input Power[1] (VSWR 20:1, 10 seconds)		40	dBm
	TX Input Power[1] (50 Ω)		45	dBm
	RX Input Power at ANT pin[2] (VSWR 20:1)		27	dBm
	RF Input Power on inactive ports or supply unbiased		27	dBm
P_D	Maximum Power Dissipation from RF Insertion Loss		2.8	W
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		2000	V

Notes: 1. Supply biased
2. Supply biased or unbiased

Absolute Maximum Ratings

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Figure 3. Pin Configuration (Top View)

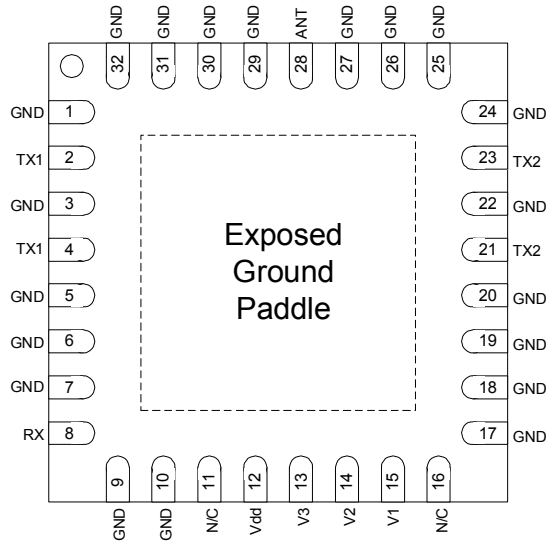


Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	TX1	TX1 port
3	GND	Ground
4	TX1[1]	TX1 port
5-7	GND	Ground
8	RX	RX port
9-10	GND	Ground
11	N/C	No Connect
12	V_{DD}	Nominal 3.3 V supply connection
13	V3	Control
14	V2	Control
15	V1[2]	Control
16	N/C	Do not connect
17-20	GND	Ground
21	TX2	TX2 port
22	GND	Ground
23	TX2[3]	TX2 port
24-27	GND	Ground
28	ANT	Antenna Port
29-32	GND	Ground
Paddle	GND	Exposed ground paddle

Note: 1. Must be tied to pin 2
2. Must be tied to V2
3. Must be tied to pin 21

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. Control Logic Truth Table

Path	V3	V2	V1
ANT – RX Attenuated	L	L	L
Unsupported mode	L	L	H
Unsupported mode	L	H	L
ANT – TX1	L	H	H
ANT – RX	H	L	L
Unsupported mode	H	L	H
Unsupported mode	H	H	L
ANT – TX2	H	H	H

End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Evaluation Kit

The PE42650A Evaluation Kit board was designed to ease customer evaluation of the PE42650A RF switch.

DC power is supplied through J10, with V_{DD} on pin 9, and GND on the entire lower row of even numbered pins. To evaluate a switch path, add or remove jumpers on V1 (pin 3), V2 (pin 5), and V3 (pin 7) using Table 5 (adding a jumper pulls the CMOS control pin low and removing it allows the on-board pull-up resistor to set the CMOS control pin high). J10 pins 1, 11, and 13 are N/C.

The RF common port (ANT) is connected through a 50 Ohm transmission line via the top SMA connector, J1. RX and TX paths are also connected through 50 Ohm transmission lines via SMA connectors. A 50 Ohm through transmission line is available via SMA connectors J8 and J9. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. An open-ended 50 Ohm transmission line is also provided at J7 for calibration if needed.

Narrow trace widths are used near each part to improve impedance matching.

Figure 4. Evaluation Board Layout

Peregrine Specification 101-0315

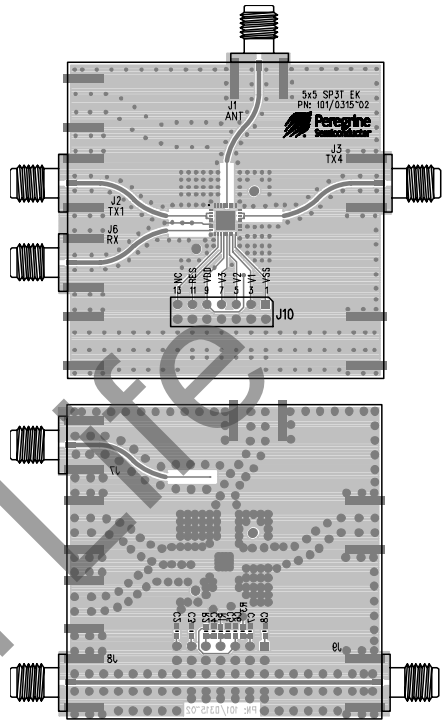
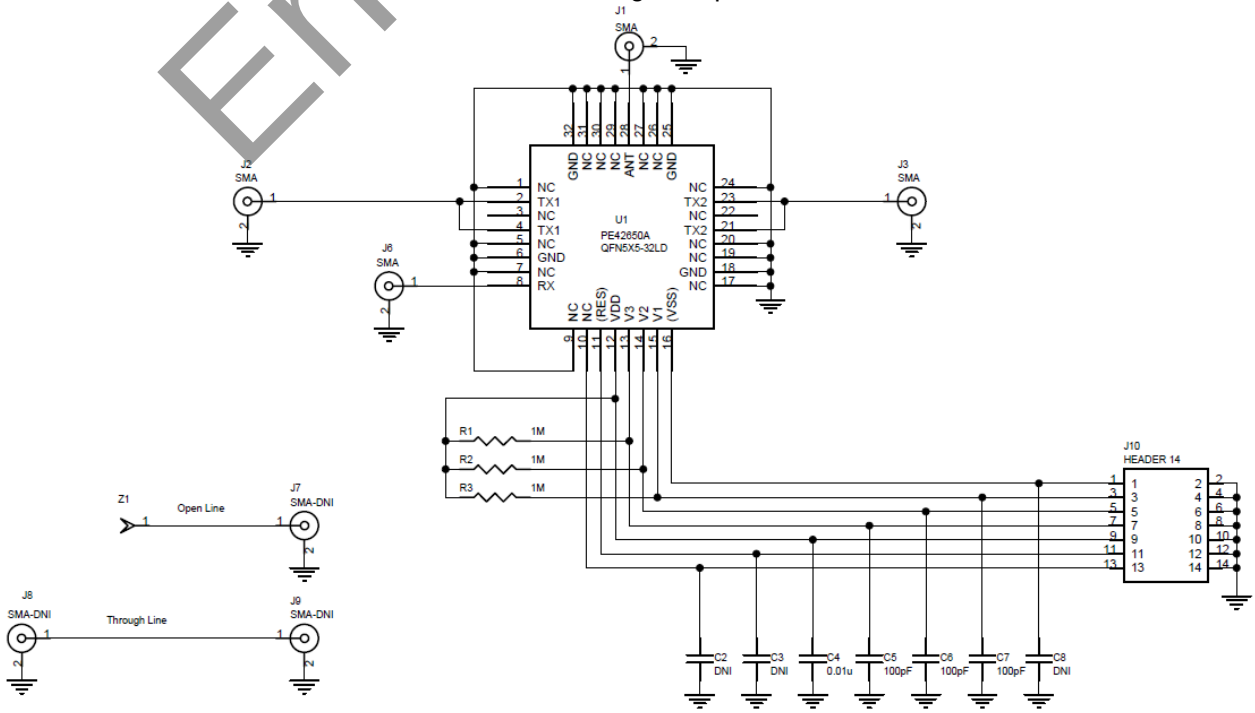


Figure 5. Evaluation Board Schematic

Peregrine Specification 102-0535



End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Performance Plots

Figure 6. Isolation, Tx-Tx, V_{DD}=3.3V

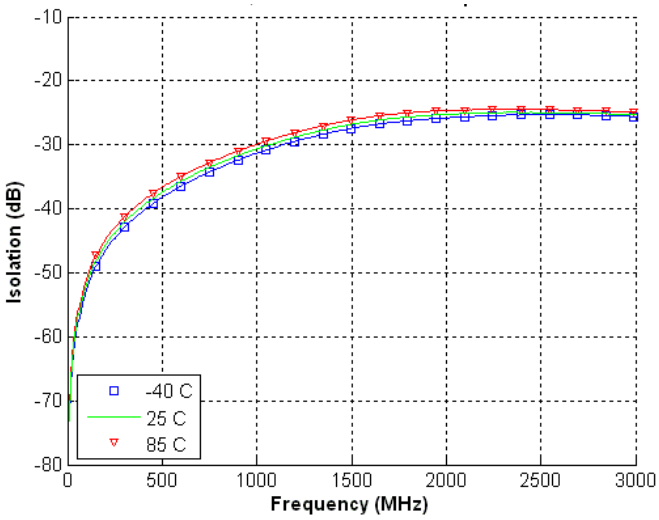


Figure 7. Isolation, Tx-Rx, V_{DD}=3.3V

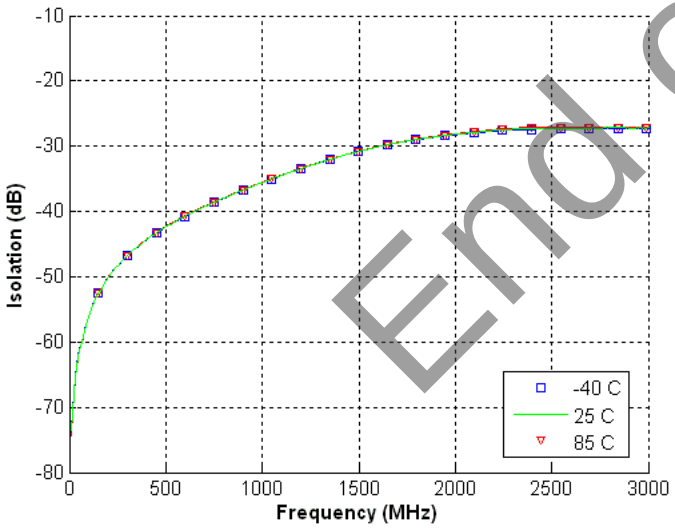


Figure 8. Isolation, Tx-Tx, +25°C

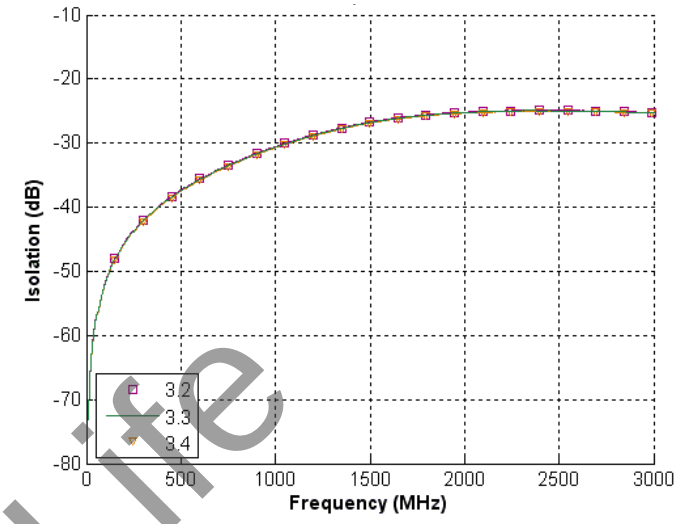
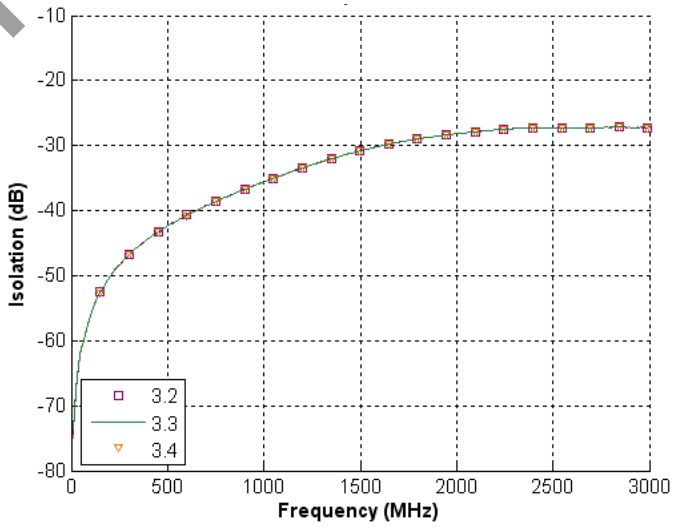


Figure 9. Isolation, Tx-Rx, +25°C



End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Figure 10. Tx Insertion Loss, V_{DD}=3.3V

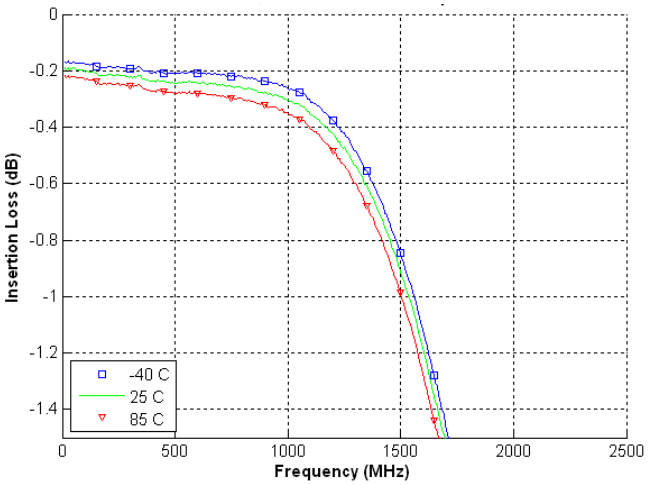


Figure 11. Rx Insertion Loss Un-Attenuated, V_{DD}=3.3V

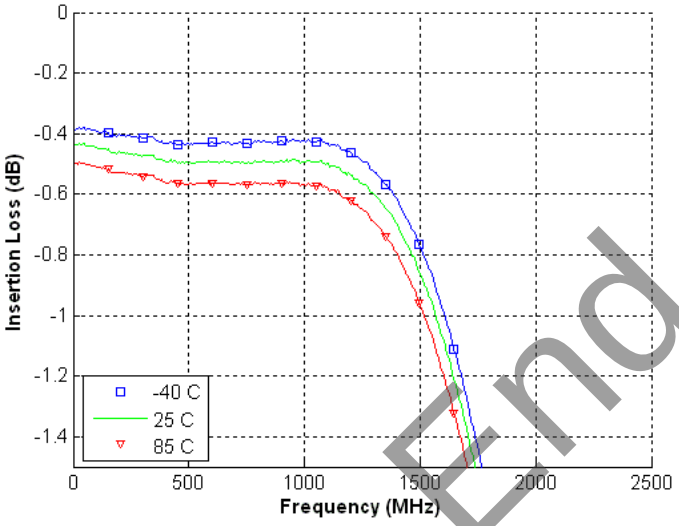


Figure 12. Rx Insertion Loss Attenuated, V_{DD}=3.3V

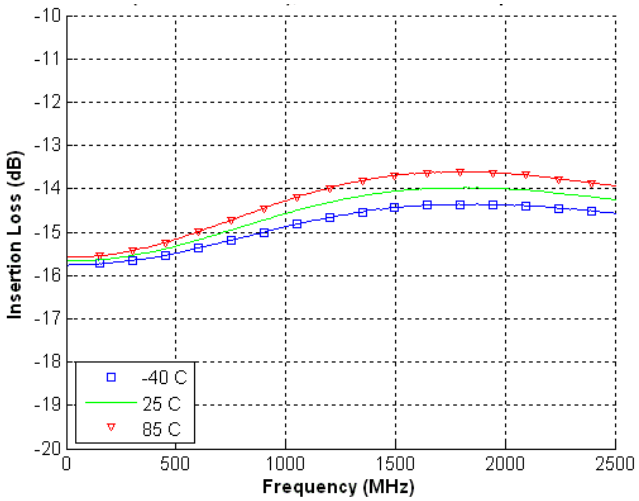


Figure 13. Tx Insertion Loss, +25°C

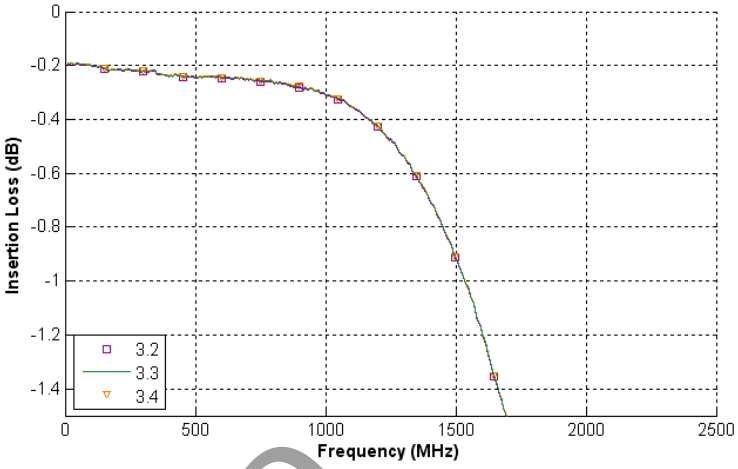


Figure 14. Rx Insertion Loss Un-Attenuated, +25°C

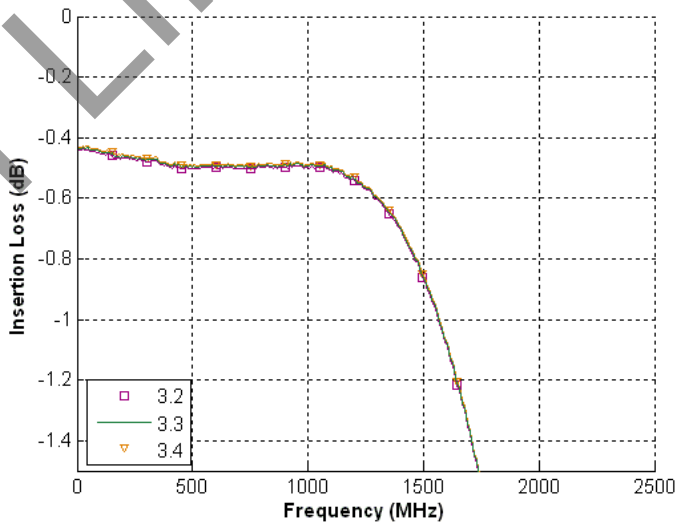
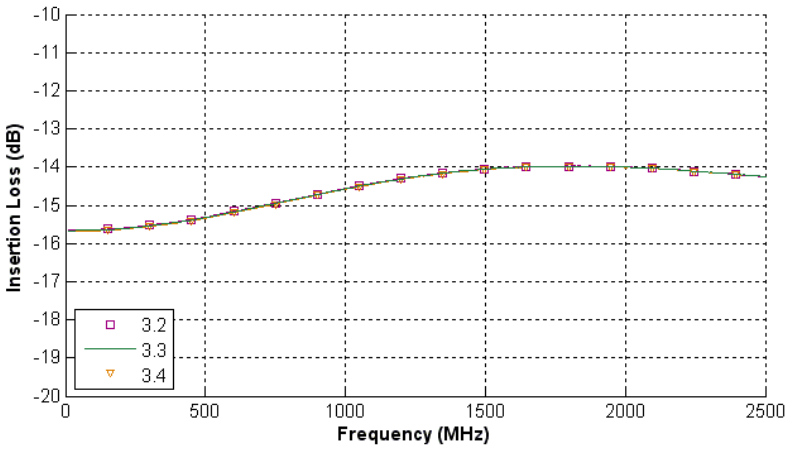


Figure 15. Rx Insertion Loss Attenuated, +25°C



End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Figure 16. Return Loss, V_{DD}=3.3V

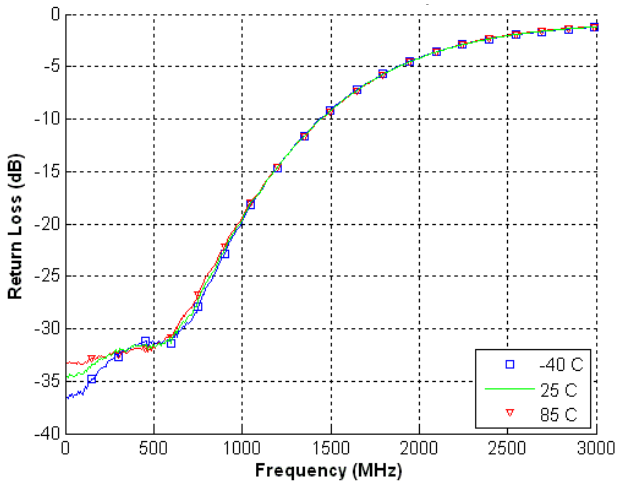


Figure 17. Tx Return Loss, V_{DD}=3.3V

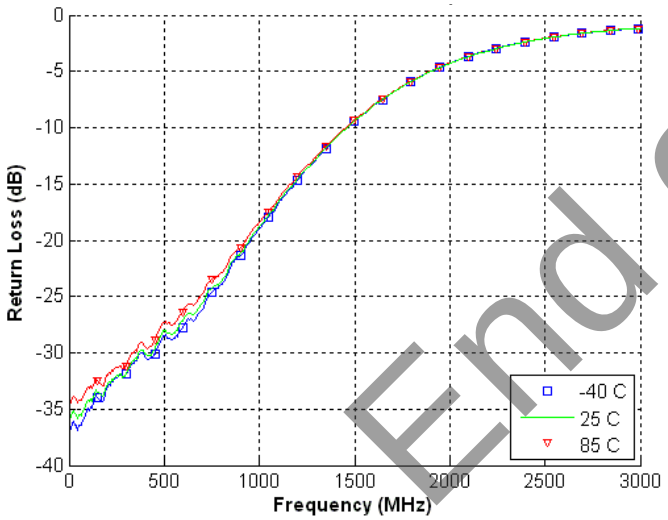


Figure 18. Return Loss, +25°C

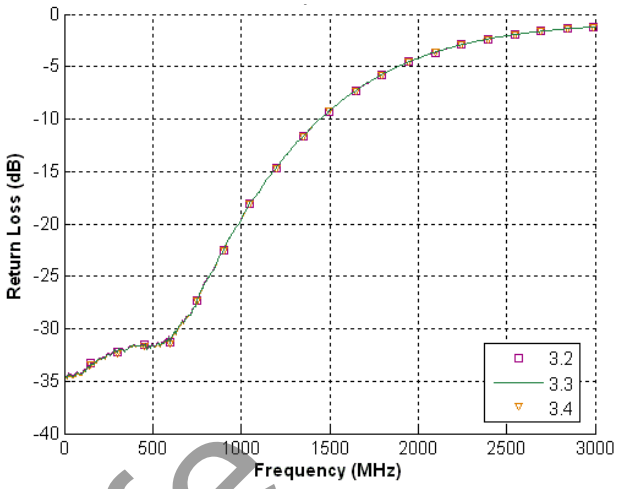
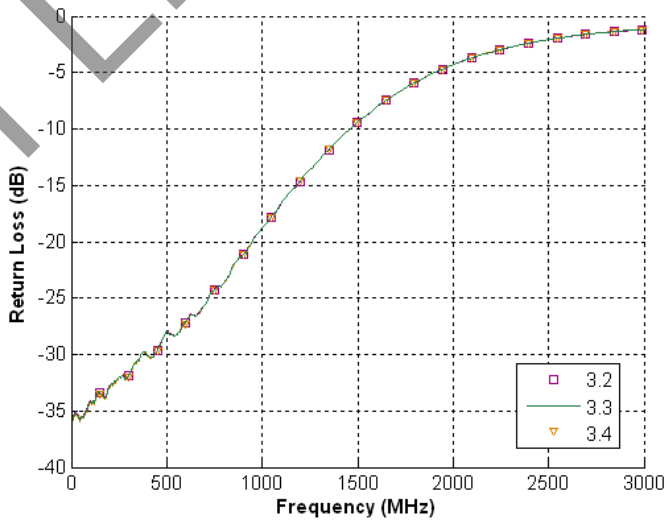


Figure 19. Tx Return Loss, +25°C



End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Figure 20. Rx Return Loss Attenuated, V_{DD}=3.3V

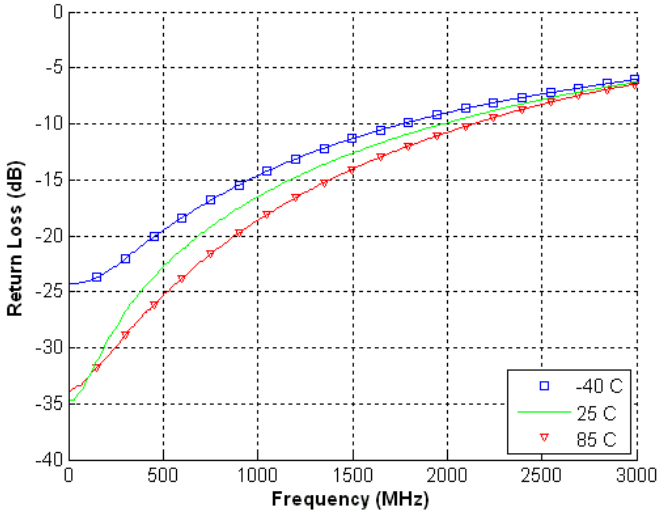


Figure 21. Rx Return Loss Un-Attenuated, V_{DD}=3.3V

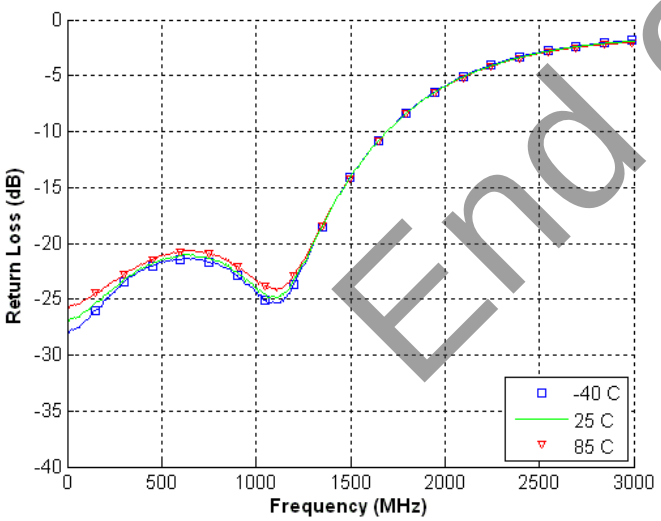


Figure 22. Rx Return Loss Attenuated, +25°C

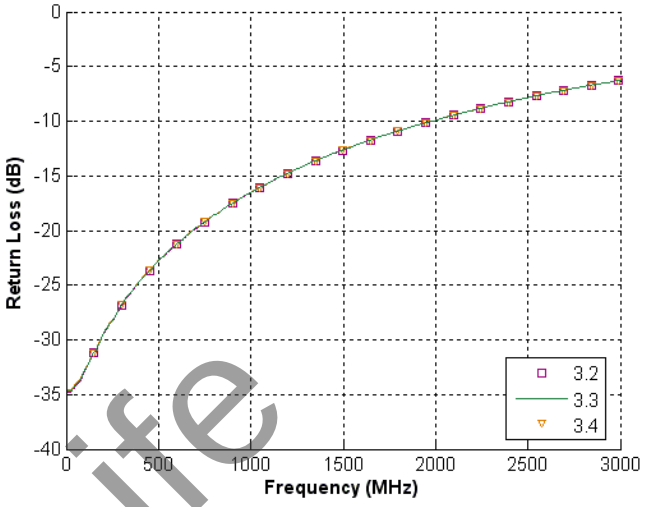
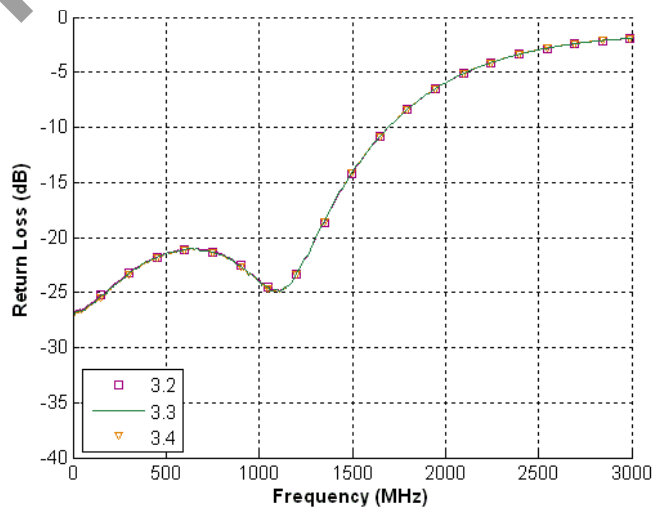


Figure 23. Rx Return Loss Un-Attenuated, +25°C



End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Thermal Data

Though the insertion loss for this part is very low, when handling high power RF signals, the part can get quite hot.

Figure 24 shows the estimated power dissipation for a given incident RF power level. Multiple curves are presented to show the effect of poor VSWR conditions. VSWR conditions that present short circuit loads to the part can cause significantly more power dissipation than with proper matching.

Figure 25 shows the estimated maximum junction temperature of the part for similar conditions.

Note that both of these charts assume that the case (GND slug) temperature is held at 85C. Special consideration needs to be made in the design of the PCB to properly dissipate the heat away from the part and maintain the 85C maximum case temperature. It is recommended to use best design practices for high power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Special care also needs to be made to alleviate solder voiding under the part.

Table 6. Theta JC

Parameter	Min	Typ	Max	Units
Theta JC (+85°C)		15		C/W

Figure 24. Power Dissipation

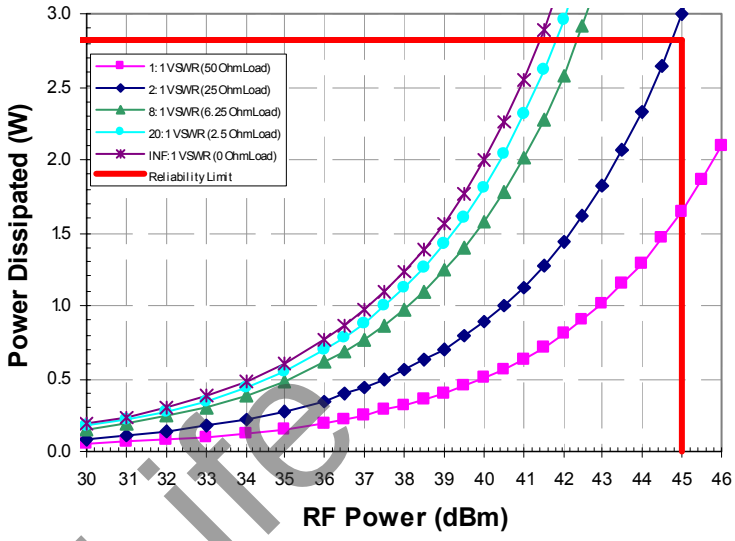
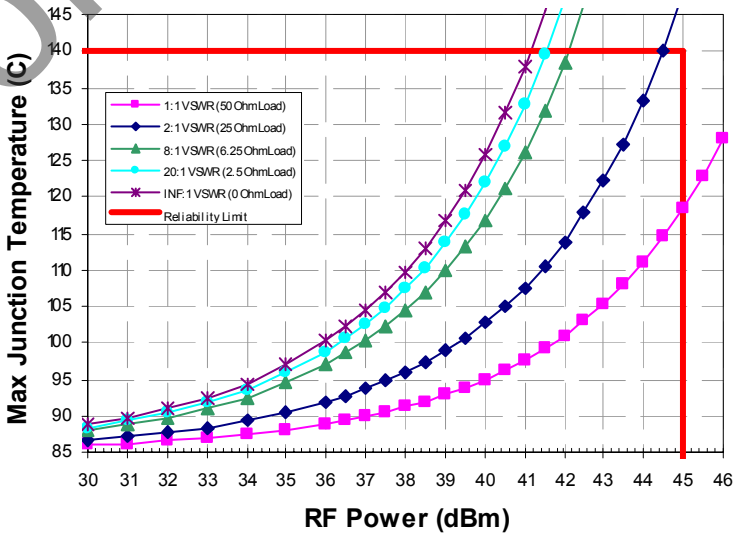


Figure 25. Maximum Junction Temperature



End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Figure 26. Package Drawing

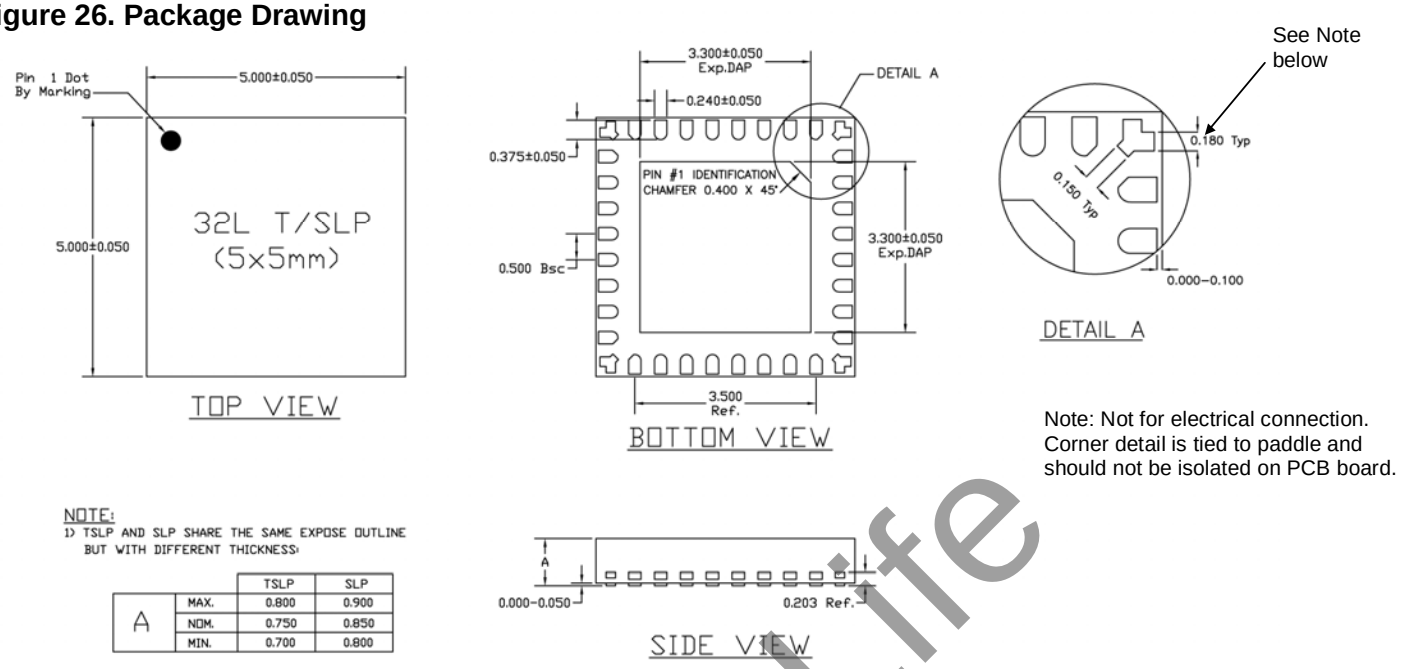
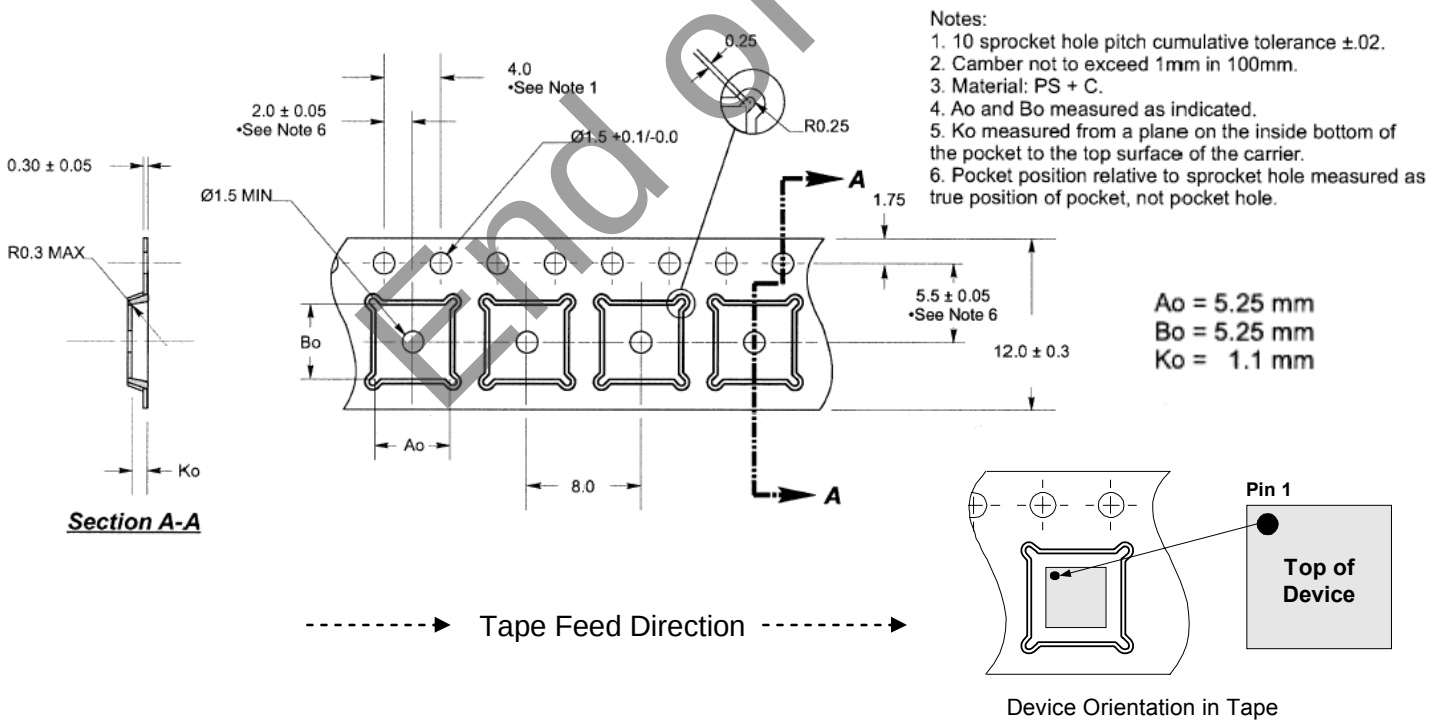


Figure 27. Tape and Reel Specs



End of Life

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
PE42650AMLI-Z	42650A	Parts on Tape and Reel	Green 32-lead 5x5mm QFN	3000 units / T&R
PE42650AMLI	42650A	Parts in Tubes or Cut Tape	Green 32-lead 5x5mm QFN	73 units / Tube
EK42650A-01	42650A	Evaluation Kit	Evaluation Kit	1 / Box

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

Sales Offices

The Americas

Peregrine Semiconductor Corporation
9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

High-Reliability and Defense Products

Americas
San Diego, CA, USA
Phone: 858-731-9475
Fax: 848-731-9499

Europe/Asia-Pacific
Aix-En-Provence Cedex 3, France
Phone: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea
#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS, HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.

End of Life

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com