High Performance, sub-GHz Radio Transceiver IC

Preliminary Technical Data

ADF7030-1

FEATURES

- Radio frequency (RF) ranges
  - 169.4 MHz to 169.6 MHz
  - 426 MHz to 470 MHz
  - 863 MHz to 960 MHz
- Data rates
  - 2FSK/2GFSK: 0.1 kbps to 300 kbps
  - 4FSK/4GFSK: 0.1 kbps to 400 kbps (transmit only)
- Dual power amplifiers (PAs)
- Programmable receiver bandwidth from 3 kHz to 487 kHz
- Receiver (Rx) performance
  - Up to 97 dB blocking at ±10 MHz offset
  - Up to 66 dB adjacent channel rejection
  - −122.8 dBm sensitivity at 2.4 kbps
- Transmitter (Tx) performance
  - −20 dBm to +17 dBm range with 0.1 dB step resolution
  - Very low output power variation vs. temperature and supply
- Low active current
  - 61 mA Tx current at 17 dBm
  - TBD mA Tx current at 10 dBm
  - 24 mA Rx current
- Ultralow sleep current
  - 10 nA with memory retained
  - Autonomous smart wake modes
- Host microprocessor interface
  - Easy to use programming interface (SPI)
  - Configurable 8-bit GPIO bus
- On-chip ARM Cortex-M0 processor for
  - Radio control and calibration
  - Packet management
  - Clear channel assessment
- IEEE802.15.4g support
  - Frame format
  - Data whitening
  - Dual-sync word detection
  - Forward error correction (FEC) and interleaving
- Suitable for systems targeting compliance with
  - ETSI EN 300 220
  - EN 54-25
  - FCC Part 15, Part 22, Part 24, Part 90, and Part 101
  - ARIB STD-T30, T67, T108, T96
- Packages
  - 6 mm × 6 mm, 40-lead LFCSP
  - 7 mm × 7 mm, 48-lead LQFP

APPLICATIONS

- IEEE 802.15.4g (MR-FSK PHY)
- Wireless M-Bus (EN 13757-4)
- Smart metering
- Security and building automation
- Active tag asset tracking
- Industrial control
- Wireless sensor networks (WSNs)

FUNCTIONAL BLOCK DIAGRAM

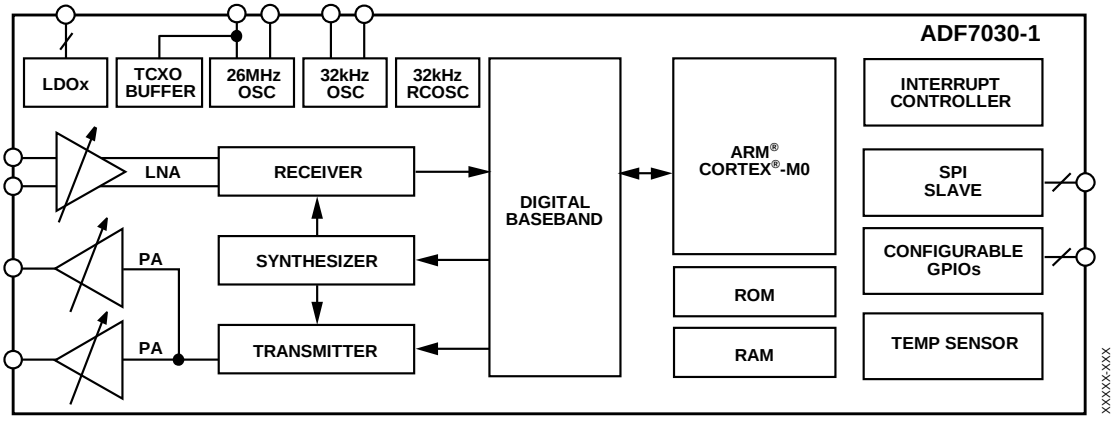

Figure 1.

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GENERAL DESCRIPTION

The ADF7030-1 is a fully integrated, radio transceiver achieving high performance at very low power. The ADF7030-1 is ideally suited for applications that require long range, network robustness, and long battery life. It is suitable for applications that operate in the ISM, SRD, and licensed frequency bands at 169 MHz, 426 MHz to 470 MHz, and 862 MHz to 960 MHz. It provides extensive support for standards-based protocols like IEEE802.15.4g while also providing flexibility to support a wide range of proprietary protocols.

The highly configurable low intermediate frequency (IF) receiver supports a large range of IF bandwidths from 3.6 kHz to 487 kHz. This allows the ADF7030-1 to support ultranarrow-band, narrow-band, and wideband channel spacing.

The ADF7030-1 features two independent PAs supporting output power ranges of −20 dBm to +13 dBm and −20 dBm to +17 dBm. The PAs support ultrafine adjustment of the power with a step resolution of 0.1 dB. The PA output power is exceptionally robust over temperature and voltage. The PAs have an automatic power ramp control to prevent spectral splatter and help meet regulatory standards.

The ADF7030-1 features an on-chip ARM® Cortex®-M0 processor that performs radio control, radio calibration, and packet management. Cortex-M0 eases the processing burden of the host processor because the ADF7030-1 integrates the lower layers of a typical communication protocol stack. This internal processor also permits the download and execution of Analog Devices, Inc., provided firmware modules that can extend the functionality of the ADF7030-1.

The ADF7030-1 has two packet modes: generic packet mode and IEEE802.15.4g mode. In generic packet mode, the packet format is highly flexible and fully programmable, thereby ensuring its compatibility with proprietary packet formats. In IEEE802.15.4g packet mode, the packet format conforms to the IEEE802.15.4g standard. FEC, as per the IEEE802.15.4g standard, is also supported.

The ADF7030-1 operates with a power supply range of 2.2 V to 3.6 V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems. An ultralow power deep sleep mode achieves a typical current of 10 nA with the configuration memory retained.

The ADF7030-1 supports smart wake mode (SWM) where the ADF7030-1 can wake up autonomously from sleep using an internal RTC without intervention from the host processor. After wake-up, the ADF7030-1 operates autonomously. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby reducing overall system current consumption. The ADF7030-1 autonomous operation can also be triggered by the Host processor using the interrupt input of the ADF7030-1.

A complete wireless solution can be built using a small number of external discrete components and a host processor (typically a microcontroller). The host processor can configure the ADF7030-1 using a simple command-based protocol over a standard 4-wire SPI interface. A single-byte command transitions the radio between states or performs a radio function.

The ADF7030-1 is available in two package types: a 6 mm × 6 mm 40-lead LFCSP and a 7 mm × 7 mm 48-lead LQFP. Both package types use NiPdAu plating to mitigate against silver migration in high humidity applications. The ADF7030-1 operating temperature range is −40°C to +85°C.

SPECIFICATIONS

V_{DD} = VBAT1 = VBAT2 = VBAT3 = VBAT4 = VBAT5 = VBAT6 = 2.2 V to 3.6 V, exposed pad (EPAD) = 0 V (ground), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C, unless otherwise noted. All VBATx pins must be tied together.

TEMPERATURE AND VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE, T_A	−40		+85	°C	
VOLTAGE SUPPLY					
VBATx Pin Voltage	2.2		3.6	V	Transmit power ≤ 13dBm
	2.85		3.6	V	Transmit power ≥ 17dBm

GENERAL RF

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF FREQUENCY					
Frequency Range	169.4		169.6	MHz	
	426		470	MHz	
	863		960	MHz	
Channel Frequency Resolution		1.5		Hz	
DATA RATE					
2FSK, 2GFSK Modulation	0.1		300	kbps	
4FSK, 4GFSK Modulation	1		400	kbps	Tx only, generic packet mode only
OOK Modulation		16.384		kbps	Tx only, Manchester encoded, generic packet mode only
Resolution		1		bps	
FREQUENCY DEVIATION					
Range					
2FSK, 2GFSK Modulation	1		250	kHz	
4FSK, 4GFSK Modulation	1		250	kHz	Tx only, generic packet mode only
Resolution		100		Hz	
GAUSSIAN FILTER BANDWIDTH TIME (BT) PRODUCT		0.3, 0.35, 0.4, 0.5			Programmable

RECEIVE

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, BIT ERROR RATE (BER)					At BER = 0.1%, AFC disabled, 0 Hz frequency error
Data Rate = 0.1 kbps		−134.5		dBm	169 MHz, frequency deviation = TBD, 2FSK
Data Rate = 2.4 kbps		−122.8		dBm	169 MHz, frequency deviation = 2.4 kHz, 2GFSK
Data Rate = 4.8 kbps		−121.4		dBm	169 MHz, frequency deviation = 2.4 kHz, 2GFSK
		−120		dBm	460 MHz, frequency deviation = 2.4 kHz, 2GFSK
		−118.5		dBm	868 MHz, frequency deviation = 2.4 kHz, 2GFSK
Data Rate = 32.768 kbps		−112		dBm	868 MHz, frequency deviation = 50 kHz, 2FSK
Data Rate = 50 kbps		−110		dBm	433 MHz, frequency deviation = 25 kHz, 2GFSK
		−109		dBm	915 MHz, frequency deviation = 25 kHz, 2GFSK
Data Rate = 100 kbps		−108		dBm	868 MHz, frequency deviation = 50 kHz, 2FSK
Data Rate = 150 kbps		−103		dBm	915 MHz, frequency deviation = 37.5 kHz, 2GFSK
Data Rate = 300 kbps		−104		dBm	915 MHz, frequency deviation = 120 kHz, 2GFSK

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM DATA RATE ERROR TOLERANCE		±0.1		%	
RECEIVER CHANNEL FILTER BANDWIDTH					Programmable
Narrow-Band Mode					
Maximum		20		kHz	
Minimum		3		kHz	
Wideband Mode					
Maximum		488		kHz	
Minimum		77		kHz	
MAXIMUM RF INPUT LEVEL		10		dBm	
RECEIVER LINEARITY					Measured at maximum receiver gain
169 MHz					
Input Third-Order Intercept (IP3)		−8.5		dBm	Receiver channel frequency = 169.43125 MHz, $f_{SOURCE1}$ = 171.35 MHz, $f_{SOURCE2}$ = 173.26875 MHz
Input Second-Order Intercept (IP2)		53		dBm	Receiver channel frequency = 169.53125 MHz, $f_{SOURCE1}$ = 171.55 MHz, $f_{SOURCE2}$ = 171.63125 MHz
1 dB Compression (P1dB)		−18.7		dBm	Receiver channel frequency = 169.43125 MHz, $f_{SOURCE1}$ = 171.43125 MHz
460 MHz					
Input IP3		TBD		dBm	TBD
Input IP2		TBD		dBm	TBD
P1dB		TBD		dBm	TBD
915 MHz					
Input IP3		−8		dBm	Receiver local oscillator (LO) frequency (f_{LO}) = 914.8 MHz, $f_{SOURCE1} = f_{LO}$ + 0.4 MHz, $f_{SOURCE2} = f_{LO}$ + 0.7 MHz
Input IP2		50		dBm	Receiver LO frequency (f_{LO}) = 920.8 MHz, $f_{SOURCE1} = f_{LO}$ + 1.1 MHz, $f_{SOURCE2} = f_{LO}$ + 1.3 MHz
P1dB		TBD		dBm	TBD
Received Signal Strength Indicator (RSSI)					Refer to the Typical Performance Characteristics section for further detail; sensitivity defined as BER = 0.1%
Narrow-Band Mode					Use case TBD
Resolution		0.25		dB	
Calibrated Absolute Accuracy					One-point offset calibration at TBD dBm
		±2		dB	−30 dBm to sensitivity +6 dB
		±TBD		dB	−30 dBm to sensitivity
Wideband Mode					Use case TBD
Resolution		0.25		dB	
Calibrated Absolute Accuracy					One-point offset calibration at TBD dBm
		±TBD		dB	−30 dBm to sensitivity +6 dB
		±TBD		dB	−30 dBm to sensitivity
FREQUENCY ERROR INDICATOR					
Resolution		TBD		kHz	
Accuracy					
Wideband Mode		TBD		kHz	
Narrow-Band Mode		TBD		Hz	
DIFFERENTIAL LOW NOISE AMPLIFIER (LNA) INPUT IMPEDANCE 40-LEAD LFCSP PACKAGE					
LNA in Rx Mode					
f = 169 MHz		78 – j20		Ω	
f = 433 MHz		69 – j25		Ω	
f = 460 MHz		68 – j25		Ω	
f = 868 MHz		56 – j29		Ω	
f = 915 MHz		55 – j30		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LNA in Tx Mode					Combined match enabled
f = 169 MHz		7 + j2		Ω	
f = 433 MHz		7 + j4		Ω	
f = 460 MHz		7 + j4		Ω	
f = 868 MHz		8 + j8		Ω	
f = 915 MHz		8 + j8		Ω	
DIFFERENTIAL LNA INPUT IMPEDANCE 48-LEAD LQFP PACKAGE					
LNA in Rx Mode					
f = 169 MHz		78 – j16		Ω	
f = 433 MHz		71 – j18		Ω	
f = 460 MHz		TBD		Ω	
f = 868 MHz		TBD		Ω	
f = 915 MHz		57 – j20		Ω	
LNA in Tx Mode					Combined match enabled
f = 169 MHz		7 + j3		Ω	
f = 433 MHz		8 + j9		Ω	
f = 460 MHz		8 + j9		Ω	
f = 868 MHz		9 + j18		Ω	
f = 915 MHz		9 + j19		Ω	

TRANSMIT

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER AMPLIFIER (PA)					
Power Amplifier 1 (PA1)					
Transmit Power					
Maximum		13		dBm	
Minimum		−20		dBm	
Transmit Power Step Resolution		0.1		dB	
Transmit Power Variation vs. Temperature		±0.15			From −40°C to +85°C, transmit power = 13 dBm
Transmit Power Variation vs. V_{DD}		±0.1			From V_{DD} = 2.2 V to V_{DD} = 3.6 V, transmit power = 13 dBm
Transmit Power Accuracy		TBD			transmit power = 13 dBm
Power Amplifier 2 (PA2)					
Transmit Power					
Maximum					The maximum output power level achievable on PA2 depends on the programmable PA LDO setting
		17		dBm	2.85 V ≤ V_{DD} ≤ 3.6 V
		13		dBm	2.2 V ≤ V_{DD} ≤ 3.6 V
Minimum		−20		dBm	
Step Resolution		0.1		dB	
Transmit Power Variation vs. Temperature		±0.1		dB	From −40°C to +85°C, transmit power = 17 dBm
Transmit Power Variation vs. V_{DD}		±0.1		dB	From V_{DD} = 2.85 V to V_{DD} = 3.6 V, transmit power = 17 dBm
Transmit Power Accuracy		TBD		dB	Transmit power = 17 dBm
PA IMPEDANCE 40-LEAD LFCSP PACKAGE					
Optimum PA Load in Transmit					
PA1					
f = 169 MHz		47 + j10		Ω	
f =433 MHz		45 + j30		Ω	
f =460 MHz		TBD		Ω	
f =868 MHz		TBD		Ω	
f =915 MHz		50 + j20		Ω	
PA2					
f =169 MHz		38 + j10		Ω	
f =433 MHz		38 + j25		Ω	
f =460 MHz		TBD		Ω	
f =868 MHz		TBD		Ω	
f =915 MHz		38 + j18.5		Ω	
PA Input Impedance While in Rx					For combined PA and LNA match design
PA1					
f =169 MHz		TBD		Ω	
f =433 MHz		TBD		Ω	
f =868 MHz		TBD		Ω	
f =915 MHz		TBD		Ω	
PA2					
f =169 MHz		TBD		Ω	
f =433 MHz		TBD		Ω	
f =868 MHz		TBD		Ω	
f =915 MHz		TBD		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PA IMPEDANCE 48-LEAD LQFP PACKAGE					
Optimum PA Load in Transmit					
PA1					
f =169 MHz		TBD		Ω	
f =433 MHz		TBD		Ω	
f =460 MHz		TBD		Ω	
f =868 MHz		TBD		Ω	
f =915 MHz		45 + j30		Ω	
PA2					
f =169 MHz		TBD		Ω	
f =433 MHz		TBD		Ω	
f =460 MHz		TBD		Ω	
f =868 MHz		TBD		Ω	
f =915 MHz		30 + j15		Ω	
PA Input Impedance While in Rx					For combined PA and LNA match design
PA1					
f =169 MHz		6 – j236		Ω	
f =433 MHz		6 – j87		Ω	
f =868 MHz		5 – j37		Ω	
f =915 MHz		5 – j34		Ω	
PA2					
f =169 MHz		6 – j169		Ω	
f =433 MHz		4 – j58		Ω	
f =868 MHz		3 – j22		Ω	
f =915 MHz		3 – j19		Ω	

CURRENT CONSUMPTION

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state transmitting a carrier
169.4 MHz to 169.6 MHz					
PA1		TBD		mA	Power = 0 dBm
		35		mA	10 dBm
		44		mA	13 dBm
PA2		61		mA	17 dBm
426 MHz to 470 MHz					
PA1		TBD		mA	0 dBm
		TBD		mA	10 dBm
		TBD		mA	13 dBm
PA2		TBD		mA	17 dBm
863 MHz to 960 MHz					
PA1		TBD		mA	0 dBm
		TBD		mA	10 dBm
		TBD		mA	13 dBm
PA2		TBD		mA	17 dBm
RECEIVE CURRENT CONSUMPTION					In the PHY_RX state, waiting for preamble
169.4 MHz to 169.6 MHz		26		mA	Narrow-band receive path
426 MHz to 470 MHz					
Data Rate = 4.8 kbps		TBD		mA	Narrow-band receive path
Data Rate = 50 kbps		TBD		mA	Wideband receive path
863 MHz to 960 MHz					
Data Rate = 5 kbps		24		mA	Narrow-band receive path
Data Rate = 12.5 kbps		22		mA	Wideband receive path
Data Rate = 50 kbps		24		mA	Wideband receive path
Data Rate = 150 kbps		25		mA	Wideband receive path
Data Rate = 300 kbps		27		mA	Wideband receive path
SLEEP CURRENT CONSUMPTION					
Deep Sleep -					
No Memory Retained		1		nA	
Memory Retained		10		nA	
Sleep					
RC OSC Running		500		nA	
XOSC running		1000		nA	

BAND SPECIFIC RECEIVE AND TRANSMIT

169 MHz

Unless otherwise noted, the configurations detailed in Table 6 are used to specify the performance of the ADF7030-1 in Table 7. All measurements are performed on the ADF7030-1 evaluation board EV-ADF70301-169BZ, unless otherwise noted. The EV-ADF70301-169BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 6. 169.4 MHz to 169.6 MHz Configurations

Configuration	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	Receiver Bandwidth (BW) (kHz)	Packet Setup for Packet-Based Testing
2.4 kbps	169.43125	2.4	2GFSK	2.4	12.5	8.7	Preamble = 0x5555, sync word = 0xF672, payload length = 20 bytes, CRC = 2 bytes
4.8 kbps	169.418750	4.8	2GFSK	2.4	12.5	10.6	Preamble = 0x5555, sync word = 0xF672, payload length = 20 bytes, CRC = 2 bytes
6.4 kbps	169.43125	6.4	4GFSK	3.2 (outer deviation)	12.5	Not applicable (Tx only)	Not applicable

Table 7. 169.4 MHz to 169.6 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 5%, AFC enabled, RF frequency error range = ±2 kHz, data rate error range = ±400 ppm
2.4 kbps Configuration		−121.2		dBm	
4.8 kbps Configuration		−119.5		dBm	
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave (CW) interferer power level increased until BER = 0.1%; AFC disabled
2.4 kbps Configuration					
Adjacent Channel (±12.5 kHz)		66		dB	
Alternate Channel (±25 kHz)		70		dB	
±2 MHz		93		dB	
±10 MHz		97		dB	
4.8 kbps Configuration					
Adjacent Channel (±12.5 kHz)		63		dB	
Alternate Channel (±25 kHz)		69		dB	
±2 MHz		93		dB	
±10 MHz		96		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
2.4 kbps Configuration					
Adjacent Channel (±12.5 kHz)		62		dB	
Alternate Channel (±25 kHz)		70		dB	
±2 MHz		93		dB	
±10 MHz		96		dB	
4.8 kbps Configuration					
Adjacent Channel (±12.5 kHz)		55		dB	
Alternate Channel (±25 kHz)		69		dB	
±2 MHz		91		dB	
±10 MHz		95		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL SELECTIVITY AND BLOCKING—ETSI EN 300 220-1 TEST METHOD					Measured as per EN 300 220-1 V2.4.1, AFC disabled
2.4 kbps Configuration					Wanted signal level = −106.7 dBm (3 dB above the reference sensitivity level)
±2 MHz		−18		dBm	
±10 MHz		−14		dBm	
4.8 kbps Configuration					Wanted signal level = −105.8 dBm (3 dB above the reference sensitivity level)
±2 MHz		−18		dBm	
±10 MHz		−14		dBm	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
2.4 kbps Configuration		−10		dB	
4.8 kbps Configuration		−10		dB	
IMAGE REJECTION				dB	Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
Calibrated		55		dB	
Uncalibrated		TBD		dB	
SPURIOUS RESPONSE REJECTION					Measured as per EN 300 220-1 V2.4.1, AFC disabled
2.4 kbps Configuration		TBD		dB	
4.8 kbps Configuration		TBD		dB	
ADJACENT CHANNEL POWER (ACP)					Measured according to ETSI EN 300 220-1 V2.4.1; spectrum analyzer settings: measurement BW = 8.5 kHz, resolution bandwidth (RBW) = 100 Hz, video bandwidth (VBW) = 300 Hz
2.4 kbps Configuration					PA1, output power = 13 dBm
Adjacent Channel		−81		dBc	
Alternate Channel		−81		dBc	
4.8 kbps Configuration					PA2, output power = 17 dBm
Adjacent Channel		−59		dBc	
Alternate Channel		−77		dBc	
6.4 kbps Configuration					PA1, output power = 13 dBm
Adjacent Channel		−68		dBc	
Alternate Channel		−79		dBc	
OCCUPIED BANDWIDTH					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: measurement BW = 8.5 kHz, RBW = 100 Hz, VBW = 300 Hz
2.4 kbps Configuration		6.3		kHz	PA1, output power = 13 dBm
4.8 kbps Configuration		7.8		kHz	PA2, output power = 17 dBm
6.4 kbps Configuration		8.1		kHz	PA1, output power = 13 dBm
MAXIMUM SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna input; RF frequency = 169.4 MHz to 169.6 MHz
Receive					
< 1 GHz		<−63		dBm	
1 GHz to 4 GHz		−50		dBm	
Transmit					PA2, output power = 17 dBm, transmitting continuous carrier wave
47 MHz to 87.5 MHz		<TBD		dBc	
87.5 MHz to 168.5 MHz		<TBD		dBc	
168.5 MHz to 170.5 MHz		−69		dBc	Excluding frequency range $f_{CHANNEL} \pm 31.25$ kHz
170.5 MHz to 862 MHz		<TBD		dBc	
862 MHz to 1 GHz		<−87		dBc	
1 GHz to 4 GHz		<−87		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 169.4 MHz to 169.6 MHz
17 dBm Output Power					PA2
Second Harmonic		−74		dBc	
Third Harmonic		−86		dBc	
Fourth Harmonic		−90		dBc	
All Other Harmonics		<−90		dBc	
13 dBm Output Power					PA1
Second Harmonic		−73		dBc	
Third Harmonic		−82		dBc	
Fourth Harmonic		−90		dBc	
All Other Harmonics		<−90		dBc	

433 MHz

Unless otherwise noted, the configuration detailed in Table 8 is used to specify the performance of the ADF7030-1 in Table 9. All measurements performed on the ADF7030-1 evaluation board EV-ADF70301-433AZ, unless otherwise noted. The EV-ADF70301-433AZ uses a separate transmit/receive match design and a 26 MHz crystal (XTAL) reference.

Table 8. 433 MHz Configurations

Configuration	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
50 kbps	433.92	50	2GFSK	25	200	TBD	Preamble = 0xAAAA, sync word = 0x543D54C, payload length = 20 bytes, CRC = 2 bytes

Table 9. 433 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 5%, AFC enabled, RF frequency error range = ±25 ppm, data rate error range = ±0.1%
50 kbps Configuration		−108		dBm	
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, image calibrated, AFC disabled
50 kbps Configuration					
Adjacent Channel (±200 kHz)		41		dB	
Alternate Channel (±400 kHz)		53		dB	
±2 MHz		74		dB	
±10 MHz		83		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
50 kbps Configuration					Image calibrated, AFC enabled
Adjacent Channel (±200 kHz)		40		dB	
Alternate Channel (±400 kHz)		52		dB	
±2 MHz		74		dB	
±10 MHz		83		dB	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
50 kbps Configuration		−10		dB	AFC enabled
IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
50 kbps Configuration					AFC enabled
Calibrated		TBD		dB	
Uncalibrated		30		dB	
ADJACENT CHANNEL POWER (ACP)					Measured according to ETSI EN 300 220-1 V2.4.1
50 kbps		TBD		dB	Configuration: 433 MHz, 50 kbps
OCCUPIED BANDWIDTH (OBW)					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings
50 kbps Configuration		90		kHz	
MAXIMUM SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna port; RF frequency = 433 MHz
Receive					
<1 GHz		TBD		dBm	
1 GHz to 4 GHz		TBD		dBm	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Transmit					PA1, output power = 10 dBm, transmitting continuous carrier wave
<1 GHz		TBD		dBc	
1 GHz to 4 GHz		TBD		dBc	
MAXIMUM HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 433 MHz, PA1, output power = 10 dBm
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
Fourth Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	

460 MHz

Unless otherwise noted, the configuration detailed in Table 10 is used to specify the performance of the ADF7030-1 in Table 11. All measurements performed on the ADF7030-1 evaluation board EV-ADF70301-460BZ unless otherwise noted. The EV-ADF70301-460BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 10. 460 MHz Configuration

Configuration	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
7.2 kbps	460	7.2	2GFSK	2.0	12.5	TBD	Preamble = 0xAAAA, sync word = 0xF672, payload length = 20 bytes, CRC = 2 bytes

Table 11. 450 MHz to 470 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 5%, RF frequency error range = ±4 ppm, data rate error range = ±2%
7.2 kbps Configuration		−118		dBm	
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, image calibrated, AFC disabled
7.2 kbps Configuration					
Adjacent Channel (±12.5 kHz)		62		dB	
Alternate Channel (±25 kHz)		68		dB	
±2 MHz		80		dB	
±10 MHz		83		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled
7.2 kbps Configuration					
Adjacent Channel (±12.5 kHz)		54		dB	
Alternate Channel (±25 kHz)		68		dB	
±2 MHz		80		dB	
±10 MHz		84		dB	
CO-CHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
7.2 kbps Configuration		10		dB	
IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
7.2 kbps Configuration					
Calibrated		TBD		dB	
Uncalibrated		30		dB	
MARGIN TO FCC PART 90 MASK D					Configuration: 460 MHz, 7.2 kbps; measured according to FCC Part 90
7.2 kbps Configuration		TBD		dB	
MAXIMUM SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna port; RF frequency = 450 MHz to 470 MHz
Rx					
<960 MHz		TBD		dBm	
960 MHz to 12.7 GHz		TBD		dBm	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Tx					PA2, output power = 17 dBm, transmitting continuous carrier wave
<960 MHz		TBD		dBc	
960 MHz to 12.7 GHz		TBD		dBc	
MAXIMUM HARMONIC EMISSIONS					Measured conductively at antenna port, transmitting continuous carrier wave; RF frequency = 450 MHz to 470 MHz, output power = 17 dBm, PA2
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
Fourth Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	

868 MHz

Unless otherwise noted, the configurations detailed in Table 12 are used to specify the performance of the ADF7030-1 in Table 13. All measurements performed on the ADF7030-1 evaluation board EV-ADF70301-868BZ, unless otherwise noted. The EV-ADF70301-868BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 12. 868 MHz Configurations

Configuration	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
4.8 kbps	868	4.8	2GFSK	TBD	12.5	TBD	Preamble = 0xAAAA, sync word = 0xF672, payload length = 20 bytes, CRC = 2 bytes
100 kbps	868	100	2FSK	50	400	TBD	Preamble =0x55555555, sync word = 0x543D54CD, payload length = 20 bytes, CRC = 2 bytes

Table 13. 868 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 5%, AFC enabled
4.8 kbps Configuration		TBD		dBm	RF frequency error range = ±3 ppm, data rate error range = ±0.1%
100 kbps Configuration		TBD		dBm	RF frequency error range = ±25 ppm, data rate error range = ±0.1%, frequency deviation error range = ± 25%
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, image calibrated, AFC disabled
4.8 kbps Configuration					
Adjacent Channel (±12.5 kHz)		54		dB	
Alternate Channel (±25 kHz)		68		dB	
±2 MHz		78		dB	
±10 MHz		88		dB	
100 kbps Configuration					
Adjacent Channel (±400 kHz)		TBD		dB	
Alternate Channel (±800 kHz)		TBD		dB	
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled
4.8 kbps Configuration					
Adjacent Channel (±12.5 kHz)		54		dB	
Alternate Channel (±25 kHz)		68		dB	
±2 MHz		78		dB	
±10 MHz		88		dB	
100 kbps Configuration					
Adjacent Channel (±400 kHz)		TBD		dB	
Alternate Channel (±800 kHz)		TBD		dB	
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
4.8 kbps Configuration		−10		dB	
100 kbps Configuration		TBD		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
4.8 kbps Configuration					
Calibrated		TBD		dB	
Un-calibrated		30		dB	
100 kbps Configuration					
Calibrated		TBD		dB	
Uncalibrated		30		dB	
ADJACENT CHANNEL POWER (ACP)					Measured according to ETSI EN 300 220-1 V2.4.1
4.8 kbps Configuration		54		dB	
100 kbps Configuration		TBD		dB	
OCCUPIED BANDWIDTH (OBW)					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings
4.8 kbps Configuration		8.5		dB	
100 kbps Configuration		175		dB	
MAXIMUM SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna input; RF Frequency = 863 MHz to 870 MHz
Rx					
< 1 GHz		TBD		dBm	
1 GHz to 4 GHz		TBD		dBm	
Tx					PA2, 17dBm output power, transmitting continuous carrier wave
< 1 GHz		TBD		dBc	
1 GHz to 4 GHz		TBD		dBc	
MAXIMUM HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 863 MHz to 870 MHz
13 dBm Output Power					PA1
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
Fourth Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	
17 dBm Output Power					PA2
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
Fourth Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	

915 MHz

Unless otherwise noted, the configurations detailed in Table 14 are used to specify the performance of the ADF7030-1 in Table 15. All measurements performed on the ADF7030-1 evaluation board EV-ADF70301-868BZ, unless otherwise noted. The EV-ADF70301-868BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 14. 902 MHz to 928 MHz Configurations

Configuration	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
915MHz_50kbps	905	50	2GFSK	25	200	TBD	IEEE802.15.4g packet format, PSDU length = 20 bytes
915MHz_150kbps	915	150	2GFSK	37.5	400	TBD	IEEE802.15.4g packet format, PSDU length = 20 bytes
915MHz_300kbps	925	300	2GFSK	TBD	600	TBD	Preamble = AAAAAAAA Sync Word = TBD Payload length = 20 bytes CRC = 2 bytes

Table 15. 902 MHz to 928 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
2GFSK SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 5%, AFC enabled, RF frequency error range = ±TBD ppm, data rate error range = ±2%
50 kbps Configuration		−107		dBm	FEC disabled
		TBD		dBm	FEC enabled
150 kbps Configuration		−101		dBm	FEC disabled
		TBD		dBm	FEC enabled
300 kbps Configuration		−102		dBm	
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, AFC disabled
50 kbps Configuration					
Adjacent Channel (±200 kHz)		TBD		dB	
Alternate Channel (±400 kHz)		TBD		dB	
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	
150 kbps Configuration					
Adjacent Channel (±400 kHz)		46		dB	
Alternate Channel (±800 kHz)		56		dB	
±2 MHz		66		dB	
±10 MHz		77		dB	
300 kbps Configuration					
Adjacent Channel (±600 kHz)		43		dB	
Alternate Channel (±1200 kHz)		54		dB	
±2 MHz		60		dB	
±10 MHz		67		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled
50 kbps Configuration					FEC disabled
Adjacent Channel (±200 kHz)		TBD		dB	
Alternate Channel (±400 kHz)		TBD		dB	
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
150 kbps Configuration					FEC disabled
Adjacent Channel (±400 kHz)		45		dB	
Alternate Channel (±800 kHz)		55		dB	
±2 MHz		64		dB	
±10 MHz		75		dB	
300 kbps Configuration					
Adjacent Channel (±600 kHz)		42		dB	
Alternate Channel (±1200 kHz)		53		dB	
±2 MHz		58		dB	
±10 MHz		65		dB	
CO-CHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
50 kbps Configuration		−10		dB	FEC disabled
150 kbps Configuration		−10		dB	FEC disabled
300 kbps Configuration		−10		dB	
IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
50 kbps Configuration					FEC disabled
Calibrated		TBD		dB	
Uncalibrated		30		dB	
150 kbps Configuration					FEC disabled
Calibrated		TBD		dB	
Uncalibrated		30		dB	
300 kbps Configuration					
Calibrated		TBD		dB	
Uncalibrated		30		dB	
ADJACENT CHANNEL POWER (ACP)					Spectrum analyzer settings: measurement bandwidth (BW) = TBD kHz, RBW = TBD Hz, VBW = TBD Hz
50 kbps Configuration					
Adjacent Channel		TBD		dBc	
Alternate Channel		TBD		dBc	
150 kbps Configuration					
Adjacent Channel		40		dBc	
Alternate Channel		60		dBc	
300 kbps Configuration					
Adjacent Channel		37.5		dBc	
Alternate Channel		68		dBc	
OCCUPIED BANDWIDTH					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: measurement BW = TBD kHz, RBW = TBD Hz, VBW = TBD Hz
50 kbps		85		kHz	
150 kbps		175		kHz	
300 kbps		450		kHz	
MAXIMUM SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna input; RF Frequency = 902 MHz to 928 MHz
Rx					
<960 MHz		TBD		dBm	
960 MHz to 12.7 GHz		TBD		dBm	
Tx					PA2, output power = 17 dBm, transmitting continuous carrier wave
<960 MHz		TBD		dBc	
960 MHz to 12.7 GHz		TBD		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 902 MHz to 928 MHz
13 dBm Output Power					PA1
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
Fourth Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	
17 dBm Output Power					PA2
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
Fourth Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	

26 MHz REFERENCE

The ADF7030-1 requires a 26 MHz reference clock. This reference can be a 26 MHz crystal oscillator operating in parallel mode and connected between the HFXTALP and HFXTALN pins. Alternatively, a 26 MHz TCXO can be dc-coupled to the HFXTALN input. A TCXO is typically used in narrow-band applications where the transmit and receive RF frequency must meet accuracies not supported by a crystal oscillator.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
26 MHz REFERENCE INPUT					A TCXO or crystal oscillator can be used as the reference
DC-Coupled External TCXO					HFXTALN pin, clipped sine wave
TCXO Frequency		26		MHz	
Peak-to-Peak Voltage Level	0.8		1.8	V	
Voltage Level with Respect to Ground	−0.1		+1.9	V	
Duty Cycle	40		60	%	
Crystal Oscillator					Parallel load resonant crystal
Crystal Frequency		26		MHz	
Maximum Crystal ESR			50	Ω	
Crystal Load Capacitance		12		pF	
HFXTALN, HFXTALP Parallel Pin Capacitance		TBD		pF	

32 kHz OSCILLATOR

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
32 kHz RC OSCIALLATOR					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		TBD		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		TBD		%/°C	
Voltage Coefficient		TBD		%/V	
Calibration time		TBD		ms	
32 kHz EXTERNAL OSCILLATOR					
Frequency		32.768		kHz	
Start-Up Time		TBD		ms	32.768 kHz crystal with TBD pF load capacitance

TEMPERATURE SENSOR

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Accuracy					Calibrated at 25°C, result averaged over 20 measurements
		±2		°C	0°C to 40°C
		±4		°C	20°C to 55°C
		±5		°C	−40°C to +85°C

DIGITAL INPUT/OUTPUT

Table 19.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS						
Input Voltage						
High	V_{INH}	$0.7 \times V_{DD}$			V	
Low	V_{INL}			$0.2 \times V_{DD}$	V	
Input Capacitance	C_{IN}		3.6		pF	
LOGIC OUTPUTS						
Output Voltage						
High	V_{OH}	$V_{DD} - 0.4$			V	I_{OH} = 500 µA
Low	V_{OL}			0.4	V	I_{OL} = 500 µA
GPIO Load				10	pF	
Maximum GPIO Drive Strength for V_{OH}			TBD		mA	
Maximum GPIO Drive Strength for V_{OL}			TBD		mA	

DIGITAL TIMING

Table 20. SPI Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	Falling edge to MISO setup time			15	ns
t_2	$\overline{CS}$ low to SCLK setup time	40			ns
t_3	SCLK high time	40			ns
t_4	SCLK low time	40			ns
t_5	SCLK period	80			ns
t_6	SCLK falling edge to MISO delay			10	ns
t_7	MOSI to SCLK rising edge setup time	5			ns
t_8	MOSI to SCLK rising edge hold time	5			ns
t_9	SCLK falling edge to $\overline{CS}$ hold time	40			ns
t_{10}	$\overline{CS}$ high time	80			ns
t_{11}	$\overline{CS}$ low to MISO high wake-up time		92		µs
t_{12}	MISO high to SCLK setup time	SCLK low time			µs
t_{13}	$\overline{RST}$ low time	TBD			ns

Timing Diagrams

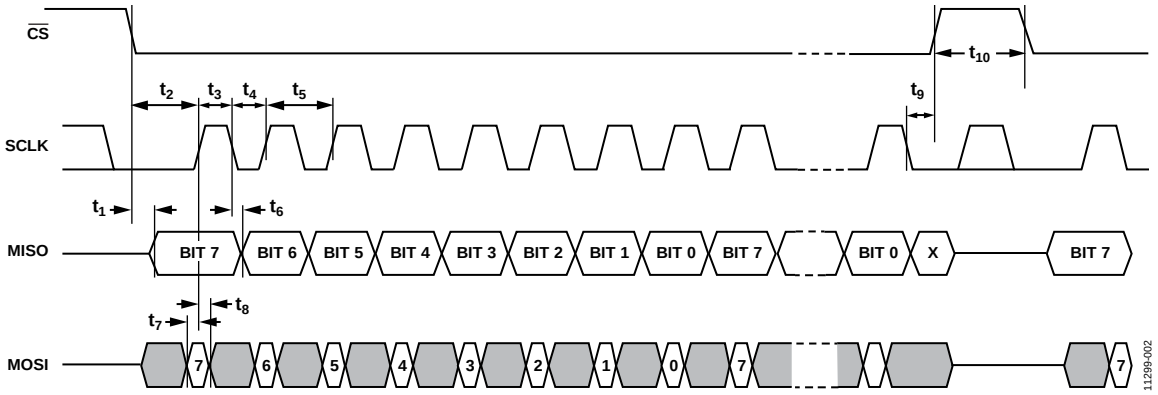


Figure 2. SPI Interface Timing

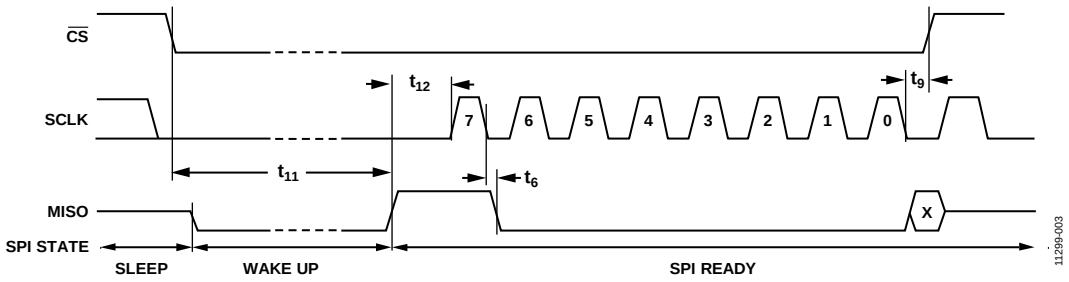


Figure 3. PHY_SLEEP to SPI Ready State Timing

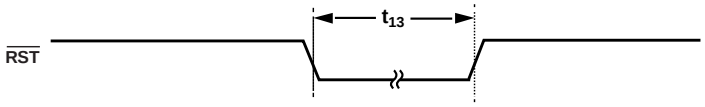


Figure 4. Reset Pin ($\overline{RST}$) Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All VBATx pins must be tied together. The LNAIN1 and LNAIN2 inputs must be ac-coupled.

Table 21. Absolute Maximum Ratings

Parameter	Rating
Supply Pins	
VBAT1, VBAT2, VBAT3, VBAT4, VBAT5, VBAT6 to Ground	−0.3 V to +3.9 V
LNAIN1, LNAIN2	−0.3 V to +1.98 V
PAOUT1, PAOUT2	−0.3 V to +3.9 V
HFXTALP, HFXTALN	−0.3 V to +1.98 V
CLF	−0.3 V to +1.98 V
CREG1, CREG2, CREG4, CREG5, CREG6, CREG7	−0.3 V to +1.98 V
CREG3	−0.3 V to +3.9 V
Digital Inputs/Outputs, GPIOx	−0.3 V to +3.9 V
MOSI, MISO, SCLK, $\overline{CS}$, $\overline{RST}$	−0.3 V to +3.9 V
Industrial Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Connect the exposed pad of the 40-lead LFCSP device to ground.

This device is a high performance, RF integrated circuit with an ESD rating of <2 kV; it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

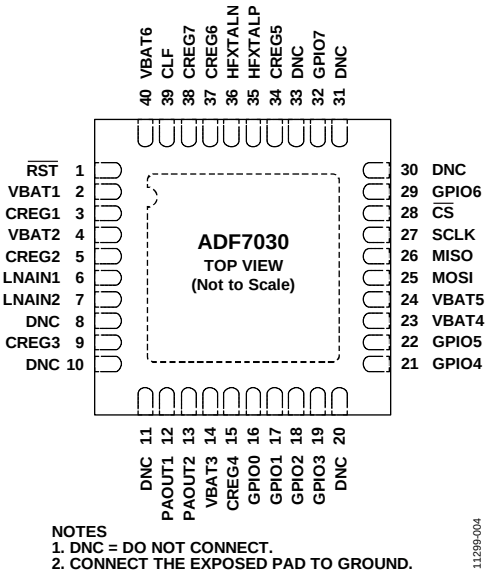
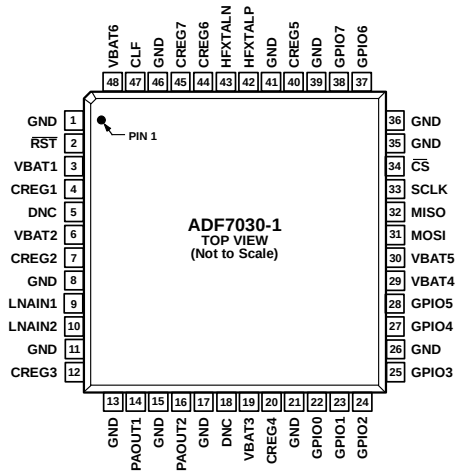


Figure 5. 40-Lead LFCSP Pin Configuration

Table 22. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{RST}$	External Reset, Active Low.
2	VBAT1	Power Supply Pin 1 to the Internal Regulators.
3	CREG1	Regulator Output 1. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. Also, place a 1.2 nF capacitor between this pin and the CLF pin.
4	VBAT2	Power Supply Pin 2 to the Internal Regulators.
5	CREG2	Regulator Output 2. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
6	LNAIN1	LNA Input 1.
7	LNAIN2	LNA Input 2.
8	DNC	Do Not Connect. Do not connect to this pin.
9	CREG3	Regulator Output 3. Connect to the PA choke inductor to provide bias to the PA. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
10	DNC	Do Not Connect. Do not connect to this pin.
11	DNC	Do Not Connect. Do not connect to this pin.
12	PAOUT1	Single-Ended PA1 Output.
13	PAOUT2	Single-Ended PA2 Output.
14	VBAT3	Power Supply Pin 3 to the Internal Regulators.
15	CREG4	Regulator Output 4. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
16	GPIO0	Digital General-Purpose Input/Output (GPIO) Pin 0.
17	GPIO1	Digital GPIO Pin 1.
18	GPIO2	Digital GPIO Pin 2.
19	GPIO3	Digital GPIO Pin 3.
20	DNC	Do Not Connect. Do not connect to this pin.
21	GPIO4	Digital GPIO Pin 4.
22	GPIO5	Digital GPIO Pin 5.
23	VBAT4	Power Supply Pin 4 to the Internal Regulators.
24	VBAT5	Power Supply Pin 5 to the Internal Regulators.
25	MOSI	Serial Port Master Output/Slave Input.
26	MISO	Serial Port Master Input/Slave Output.
27	SCLK	Serial Port Clock.
28	$\overline{CS}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7030-1 from sleep.

Pin No.	Mnemonic	Description
29	GPIO6	Digital GPIO Pin 6.
30	DNC	Do Not Connect. Do not connect to this pin.
31	DNC	Do Not Connect. Do not connect to this pin.
32	GPIO7	Digital GPIO Pin 7.
33	DNC	Do Not Connect. Do not connect to this pin.
34	CREG5	Regulator Output 5. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
35	HFXTALP	Positive Reference Input. If a 26 MHz TCXO is used as the external reference, do not connect this pin. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL.
36	HFXTALN	Negative Reference Input. If a 26 MHz TCXO is used as the external reference, connect this pin to the TCXO output. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL.
37	CREG6	Regulator Output 6. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
38	CREG7	Regulator Output 7. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
39	CLF	External Loop Filter Capacitor to CREG1. Place a 1.2 nF capacitor between this pin and the CREG1 pin.
40	VBAT6	Power Supply Pin 6 to the Internal Regulators.
	EPAD	Exposed Pad. Connect the exposed pad to ground.



NOTES
1. DNC = DO NO CONNECT.
2. CONNECT THE EXPOSED PAD TO GROUND

Figure 6. 48-Lead LQFP Pin Configuration

Table 23. 48-Lead LQFP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Connection to Ground.
2	$\overline{\text{RST}}$	External Reset, Active Low.
3	VBAT1	Power Supply Pin 1 to the Internal Regulators.
4	CREG1	Regulator Output 1. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. Also, place a 1.2 nF capacitor between this pin and the CLF pin.
5	DNC	Do Not Connect. Do not connect to this pin.
6	VBAT2	Power Supply Pin 2 to the Internal Regulators.
7	CREG2	Regulator Output 2. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
8	GND	Connection to Ground.
9	LNAIN1	LNA Input 1.
10	LNAIN2	LNA Input 2.
11	GND	Connection to Ground.
12	CREG3	Regulator Output 3. Connect to the PA choke inductor to provide bias to the PA. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
13	GND	Connection to Ground.
14	PAOUT1	Single-Ended PA1 Output.
15	GND	Connection to Ground.
16	PAOUT2	Single-Ended PA2 Output.
17	GND	Connection to Ground.
18	DNC	Do Not Connect. Do not connect to this pin.
19	VBAT3	Power Supply Pin 3 to the Internal Regulators.
20	CREG4	Regulator Output 4. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
21	GND	Connection to Ground.
22	GPIO0	Digital GPIO Pin 0.
23	GPIO1	Digital GPIO Pin 1.
24	GPIO2	Digital GPIO Pin 2.
25	GPIO3	Digital GPIO Pin 3.
26	GND	Connection to Ground.
27	GPIO4	Digital GPIO Pin 4.
28	GPIO5	Digital GPIO Pin 5.
29	VBAT4	Power Supply Pin 4 to the Internal Regulators.
30	VBAT5	Power Supply Pin 5 to the Internal Regulators.
31	MOSI	Serial Port Master Output/Slave Input.
32	MISO	Serial Port Master Input/Slave Output.

33	SCLK	Serial Port Clock.
34	$\overline{CS}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7030-1 from sleep.
35	GND	Connection to Ground.
36	GND	Connection to Ground.
37	GPIO6	Digital GPIO Pin 6.
38	GPIO7	Digital GPIO Pin 7.
39	GND	Connection to Ground.
40	CREG5	Regulator Output 5. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
41	GND	Connection to Ground.
42	HFXTALP	Positive Reference Input. If a 26 MHz TCXO is used as the external reference, do not connect this pin. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL.
43	HFXTALN	Negative Reference Input. If a 26 MHz TCXO is used as the external reference, connect this pin to the TCXO output. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL.
44	CREG6	Regulator Output 6. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
45	CREG7	Regulator Output 7. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
46	GND	Connection to Ground.
47	CLF	External Loop Filter Capacitor to CREG1. Place a 1.2 nF capacitor between this pin and the CREG1 pin.
48	VBAT6	Power Supply Pin 6 to the Internal Regulators.

TYPICAL PERFORMANCE CHARACTERISTICS

169 MHZ—RECEIVE

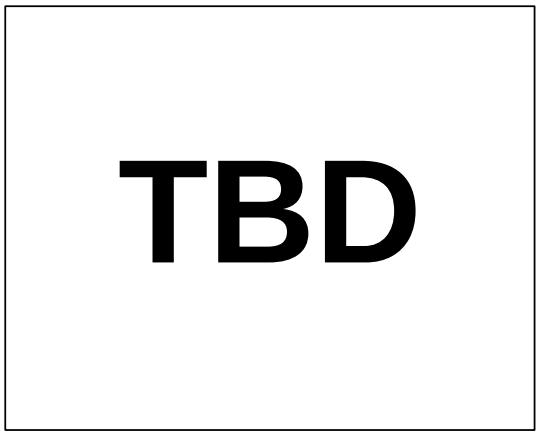


Figure 7. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration: 169 MHz, 2.4 kbps; AFC Enabled; V_{DD} = 3.0 V; T_A = 25°C

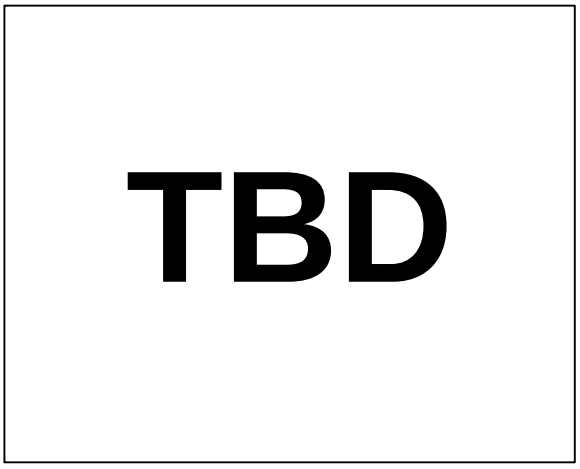


Figure 8. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration: 169 MHz, 4.8 kbps; AFC Enabled; V_{DD} = 3.0 V; T_A = 25°C

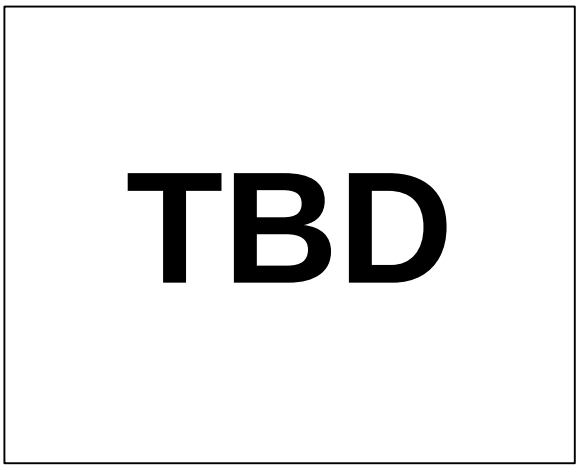


Figure 9. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}; Configuration: 169 MHz, 2.4 kbps; AFC Disabled

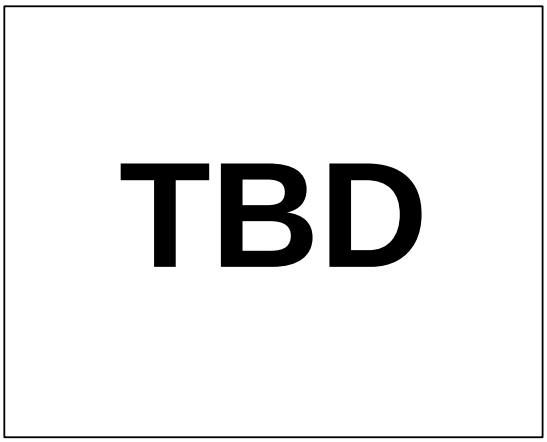


Figure 10. Receiver Close-In Blocking vs. Temperature and V_{DD}; Configuration: 169 MHz, 2.4 kbps; CW Intererer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%; BER-Based Test

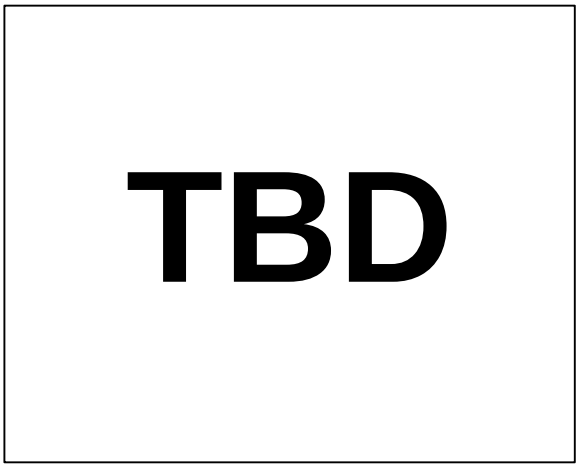


Figure 11. Receiver Wideband Blocking vs. Temperature and V_{DD}, Configuration: 169 MHz, 2.4 kbps; CW Interferer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%; BER-Based Test

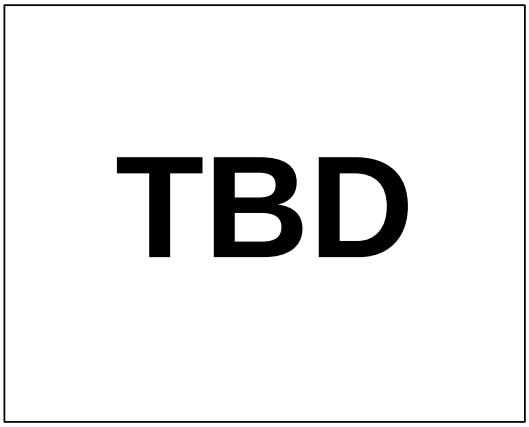


Figure 12. Packet RSSI Error vs. RF Input Power with One-Point Calibration at –70 dBm, V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

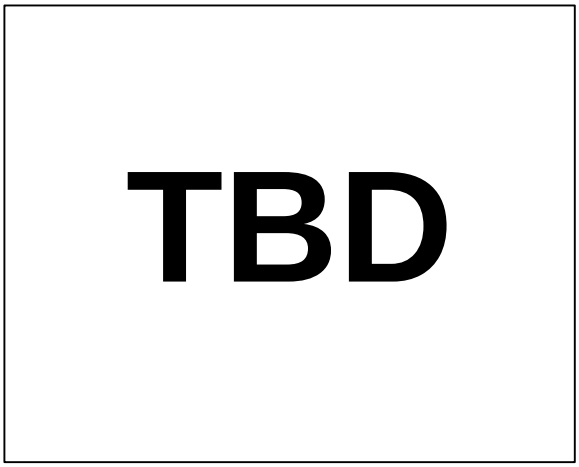


Figure 13. Receiver Wideband Blocking vs. Temperature and V_{DD}, Configuration: 169 MHz, 2.4 kbps; CW Interferer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

169 MHZ—TRANSMIT

PA_COARSE is a programmable value that provides a coarse adjustment of the PA output power. This value can be programmed in the range of 1 to 6 for PA1, and from 1 to 10 for PA2. PA_FINE is a programmable value that provides a fine adjustment of the PA output power. This value can be programmed in the range of 2 to 127 for both PA1 and PA2. PA_MICRO is a programmable value that provides a microadjustment (typically <0.1 dB) of the PA output power. This value can be programmed in the range of 1 to 31 for both PA1 and PA2.

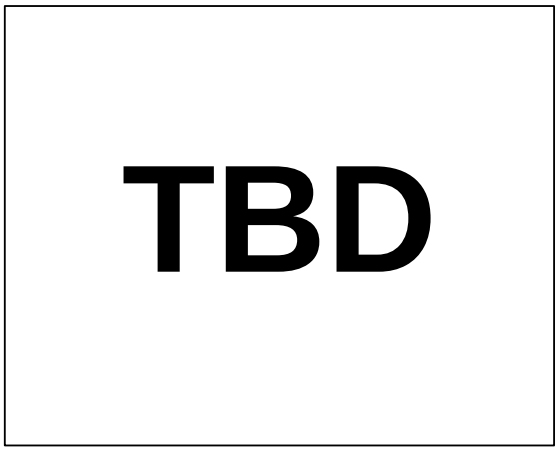


Figure 14. Phase Noise vs. Frequency Offset, RF Frequency = 169 MHz, PA2 Output Power = 17 dBm, V_{DD} = 3.0 V, T_A = 25°C

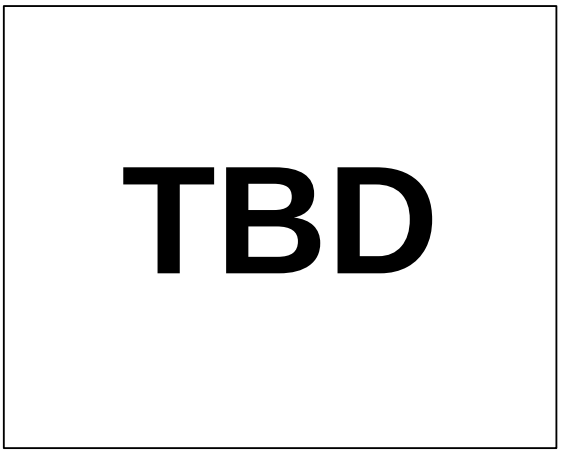


Figure 17. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, V_{DD} = 3.0 V, T_A = 25°C

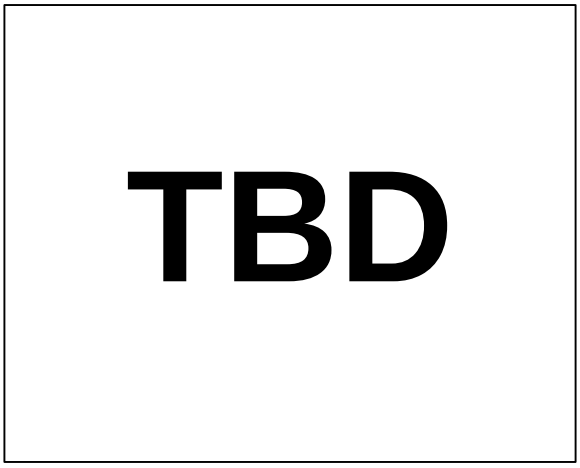


Figure 15. PA1 Output Power vs. PA_FINE Setting, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 169 MHz

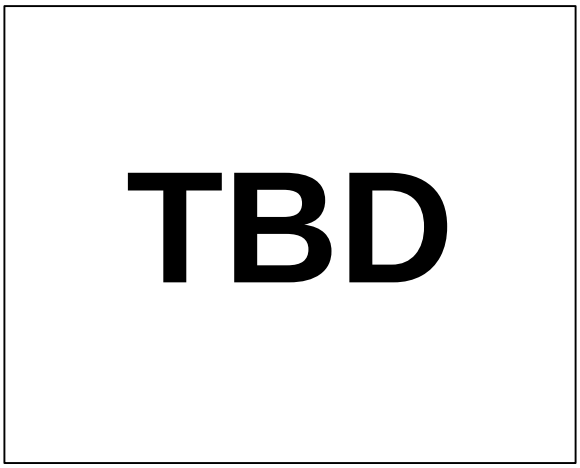


Figure 18. PA2 Output Power vs. PA_FINE Setting, Temperature, and V_{DD}, PA_COARSE = 6, RF Frequency = 169 MHz

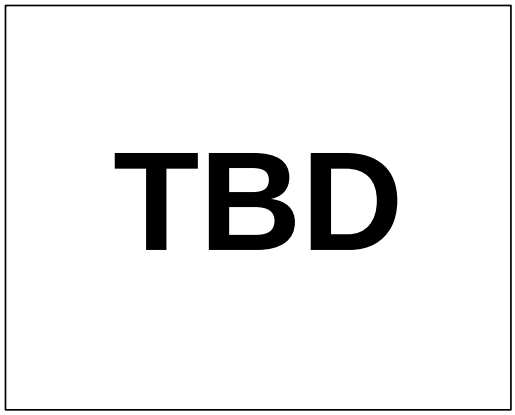


Figure 16. VBATx Supply Current vs. PA1 Output Power, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 169 MHz

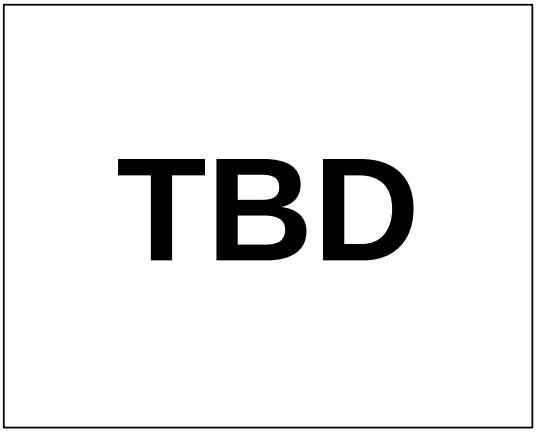


Figure 19. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD}, PA_COARSE = 10, RF Frequency = 169 MHz

PA_COARSE is a programmable value that provides a coarse adjustment of the PA output power. This value can be programmed in the range of 1 to 6 for PA1, and from 1 to 10 for PA2. PA_FINE is a programmable value that provides a fine adjustment of the PA output power. This value can be programmed in the range of 2 to 127 for both PA1 and PA2. PA_MICRO is a programmable value that provides a microadjustment (typically <0.1 dB) of the PA output power. This value can be programmed in the range of 1 to 31 for both PA1 and PA2.

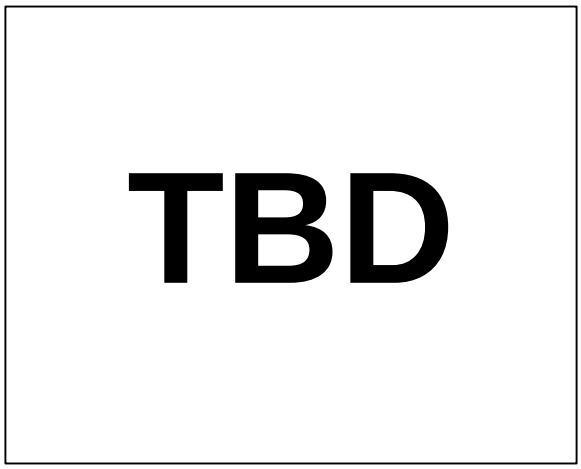


Figure 20. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, V_{DD} = 3.0 V, T_A = 25°C, RF Frequency = 169 MHz

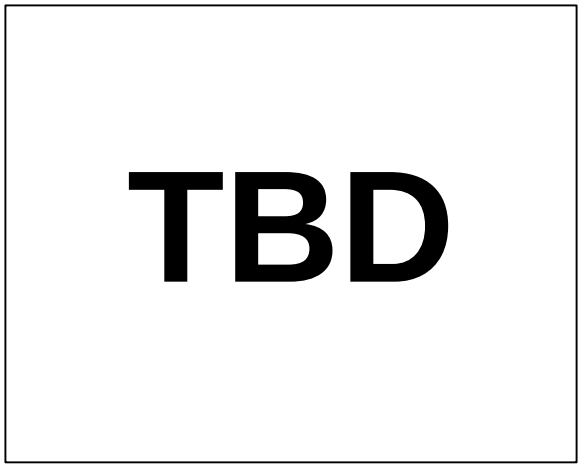


Figure 21. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 169 MHz, V_{DD} = 3.0 V, T_A = 25°C

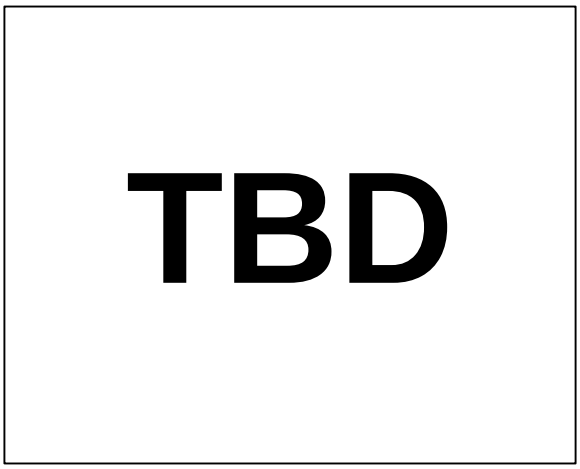


Figure 22. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 169 MHz, Data Rate = 2.4 kbps, Frequency Deviation = 2.4 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

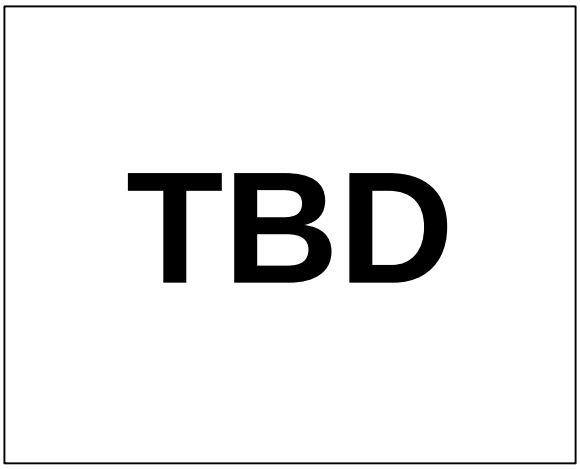


Figure 23. Transmit Spectrum, PA2 Output Power = 17 dBm, RF Frequency = 169 MHz, Data Rate = 2.4 kbps, Frequency Deviation = 2.4 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

433 MHZ—RECEIVE

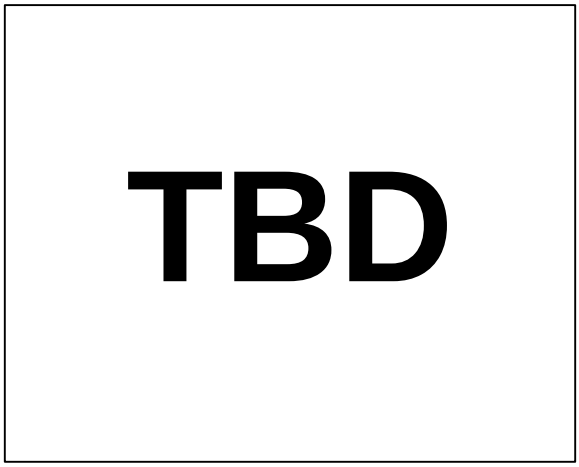


Figure 24. Packet Error Rate vs. RF Frequency Error and RF Input Power;, Configuration: 433 MHz, 50 kbps, AFC Enabled; V_{DD} = 3.0 V; T_A = 25°C

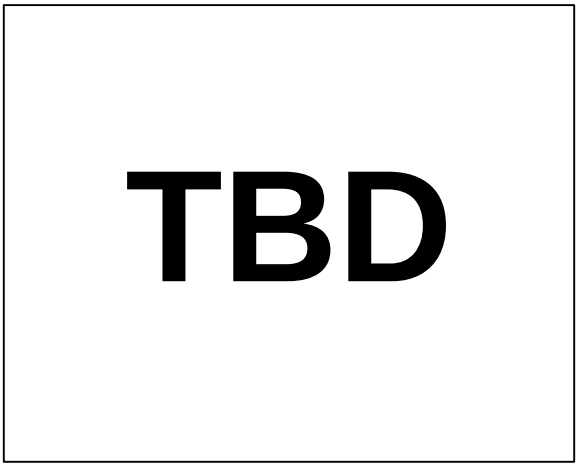


Figure 27. Receiver Wideband Blocking vs. Temperature and V_{DD}; Configuration: 433 MHz, 50 kbps; CW Interferer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%; BER-Based Test

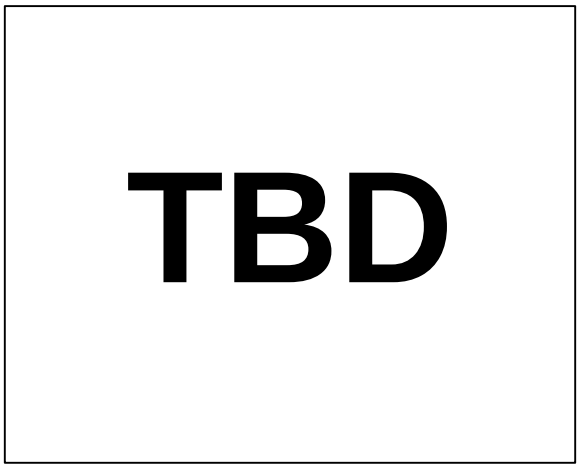


Figure 25. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}; Configuration: 43 3MHz, 50 kbps; AFC Disabled

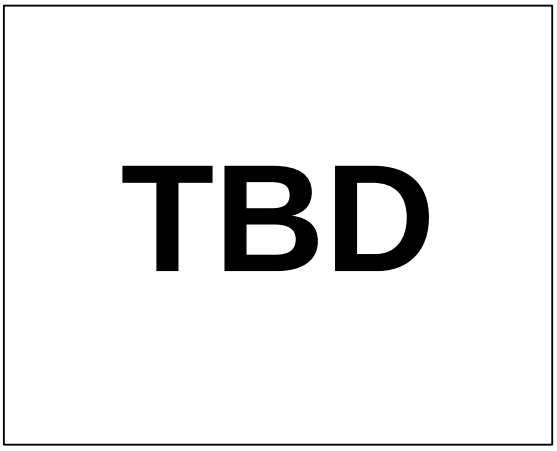


Figure 28. Packet RSSI Error vs. RF Input Power with One-Point Calibration at −70 dBm; Configuration: 433 MHz, 50 kbps; V_{DD} = 3.0 V; T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

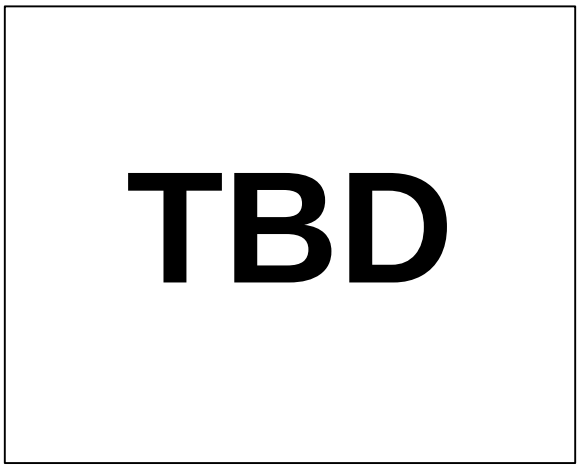


Figure 26. Receiver Close-In Blocking vs. Temperature and V_{DD}; Configuration: 433 MHz, 50 kbps; CW Interferer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%; BER-Based Test

433 MHZ—TRANSMIT

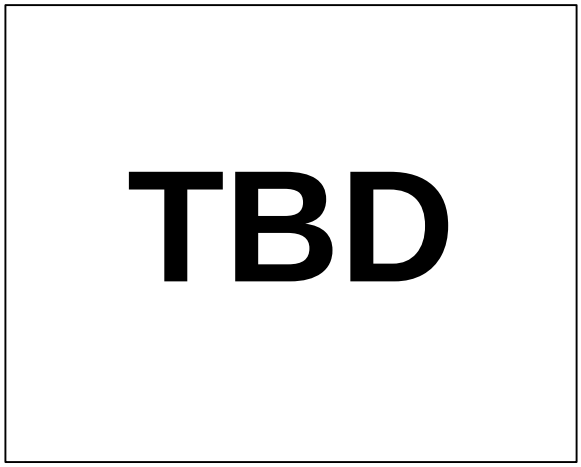


Figure 29. Phase Noise vs. Frequency Offset, RF Frequency = 433 MHz, PA1 Output Power = 10 dBm, V_{DD} = 3.0 V, T_A = 25°C

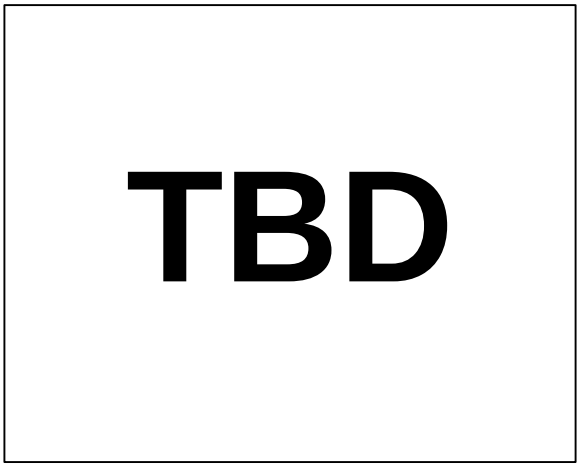


Figure 32. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, RF Frequency = 433 MHz, V_{DD} = 3.0 V, T_A = 25°C

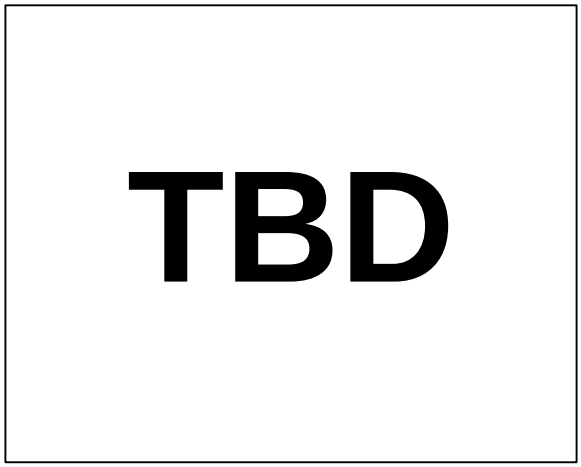


Figure 30. PA1 Output Power vs. PA_FINE Setting, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 433 MHz

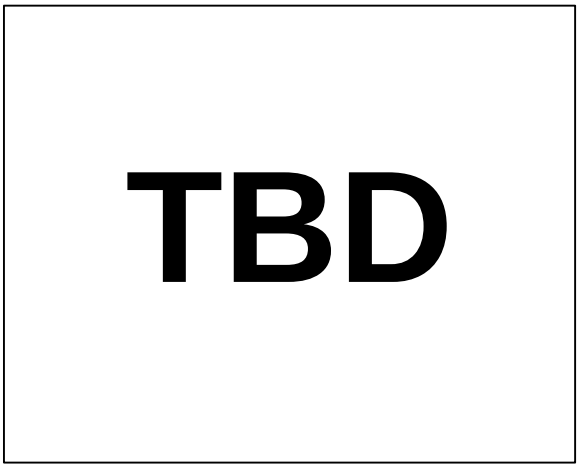


Figure 33. Conductive Harmonic Emission Level, PA1 Output Power = 10 dBm, RF Frequency = 433 MHz, V_{DD} = 3.0 V, T_A = 25°C

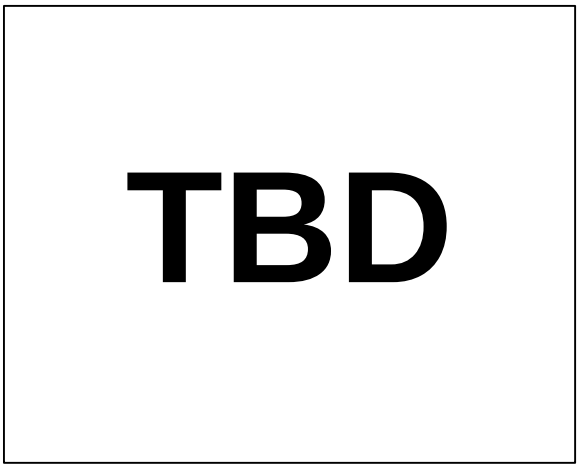


Figure 31. VBATx Supply Current vs. PA1 Output Power, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 433 MHz

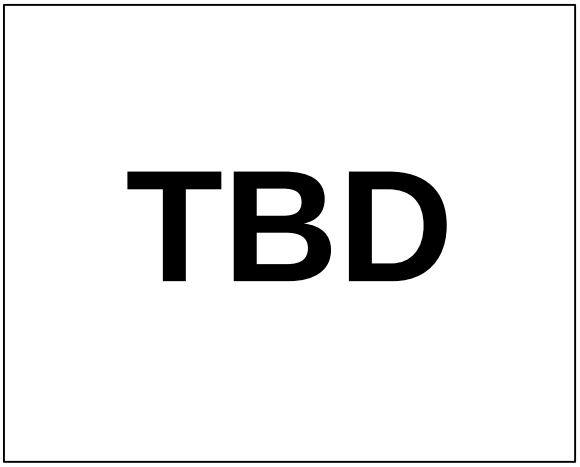


Figure 34. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 433 MHz, Data Rate = 50kbps, Frequency Deviation = 25 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

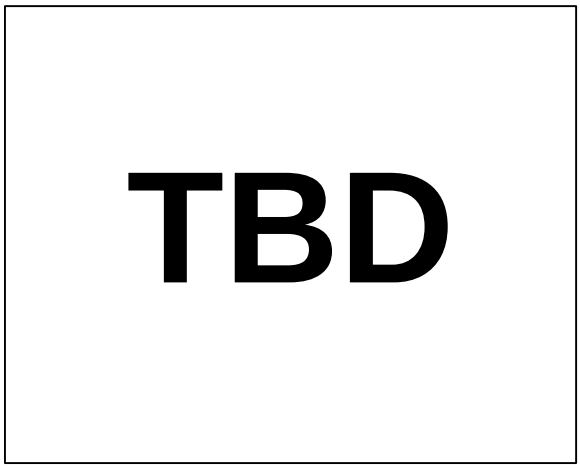


Figure 35. Transmit Spectrum, PA1 Output Power = 10 dBm, RF Frequency = 433 MHz, Data Rate = 50 kbps, Frequency Deviation = 25 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

460 MHZ—RECEIVE

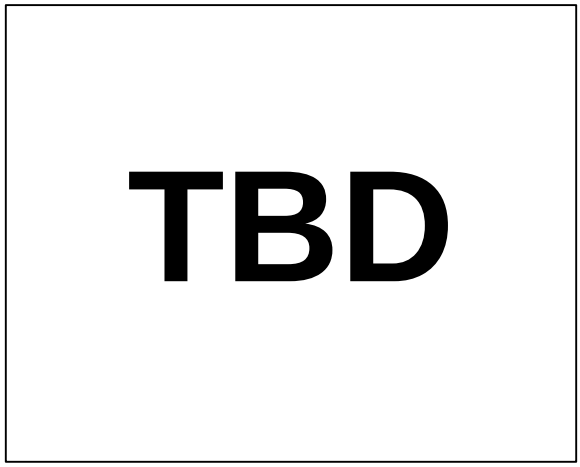


Figure 36. Packet Error Rate vs. RF Frequency Error and RF Input Power; Configuration: 460 MHz, 7.2 kbps; AFC Enabled; V_{DD} = 3.0 V; T_A = 25°C

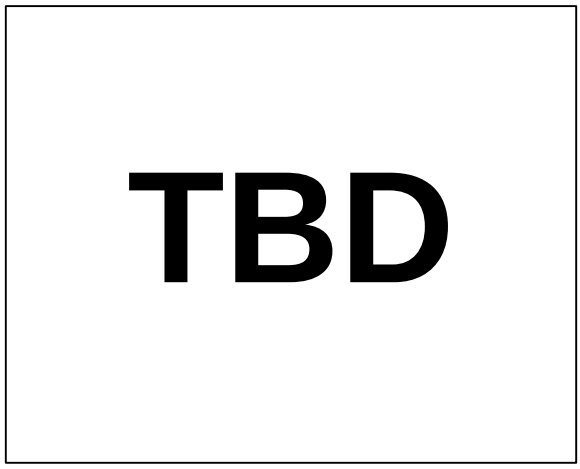


Figure 37. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}; Configuration: 460 MHz, 7.2 kbps; AFC Disabled

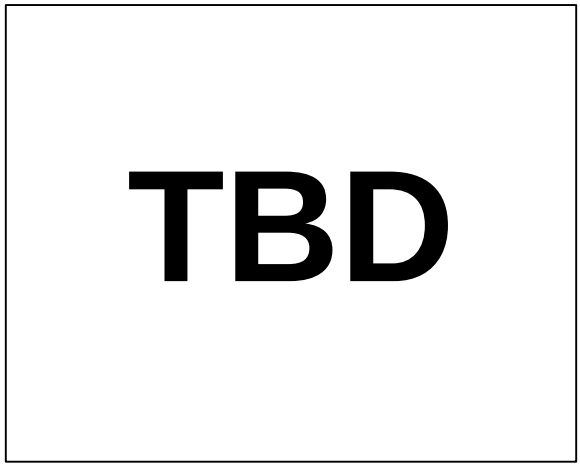


Figure 38. Receiver Close-In Blocking vs. Temperature and V_{DD}; Configuration: 460 MHz, 7.2 kbps; CW Interferer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%; BER-Based Test

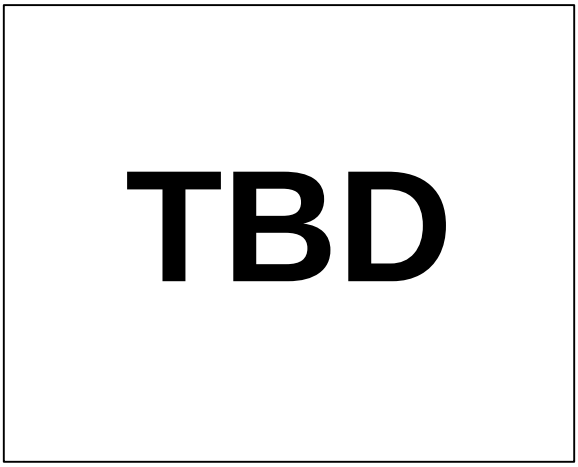


Figure 39. Receiver Wideband Blocking vs. Temperature and V_{DD}; Configuration: 460 MHz, 7.2 kbps; CW Interferer; Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%; BER-Based Test

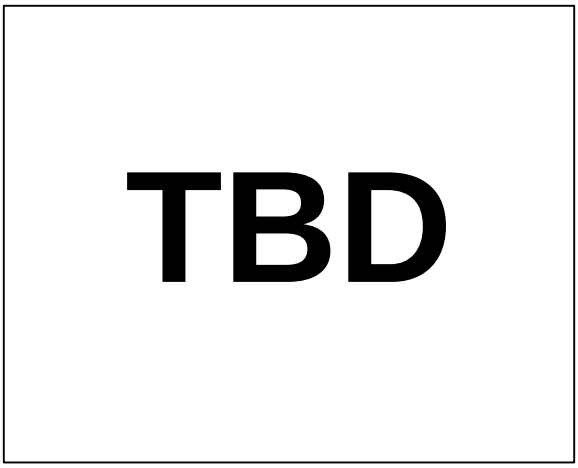


Figure 40. Packet RSSI Error vs. RF Input Power with One-Point Calibration at −70 dBm; Configuration: 460 MHz, 7.2 kbps; V_{DD} = 3.0 V; T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

460 MHZ—TRANSMIT

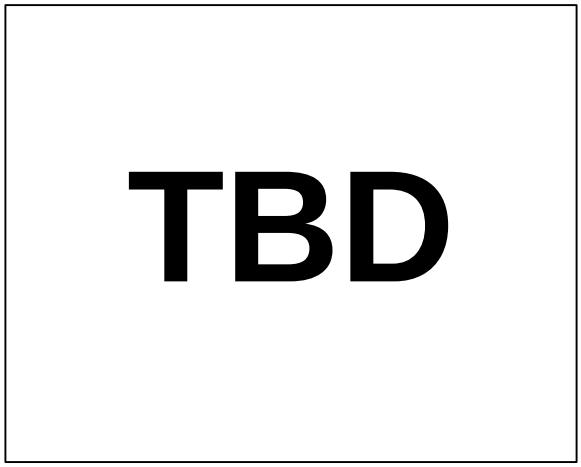


Figure 41. Phase Noise vs. Frequency Offset, RF Frequency = 460 MHz, PA2 Output Power = 17 dBm, V_{DD} = 3.0 V, T_A = 25°C

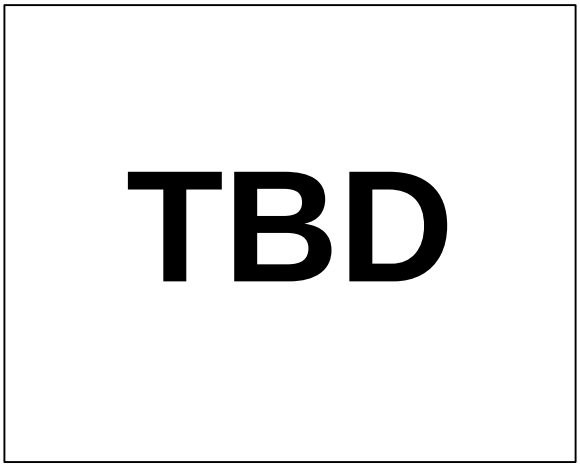


Figure 44. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, RF Frequency = 460 MHz, V_{DD} = 3.0 V, T_A = 25°C

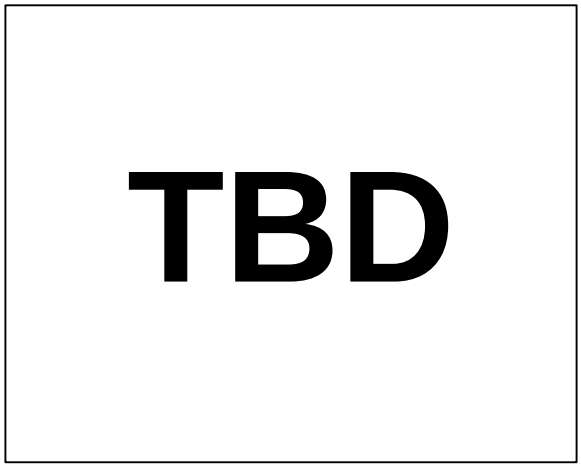


Figure 42. PA2 Output Power vs. PA_FINE Setting, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 460 MHz

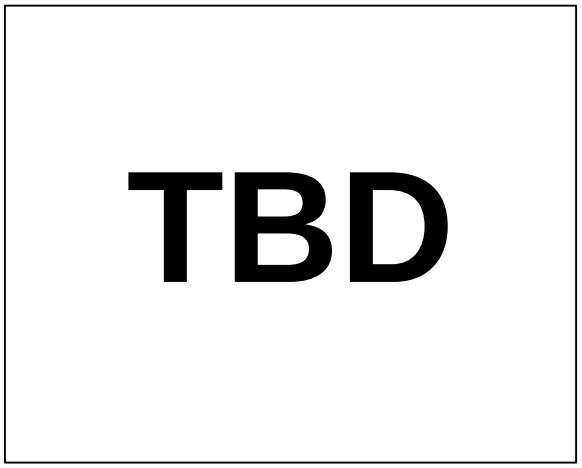


Figure 59. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 460 MHz, V_{DD} = 3.0 V, T_A = 25°C

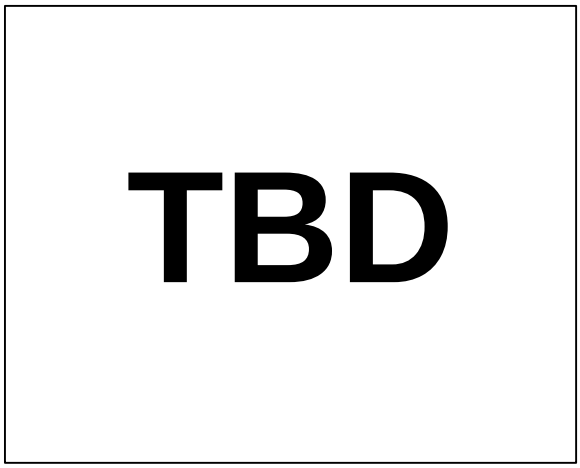


Figure 43. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 460 MHz

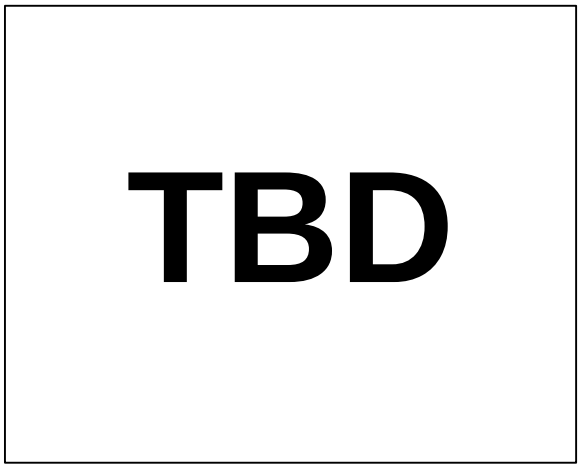


Figure 45. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 460 MHz, Data Rate = 7.2 kbps, Frequency Deviation = 2.0 kHz, Modulation = 2GFSK, BT = 0.5, V_{DD} = 3.0 V, T_A = 25°C

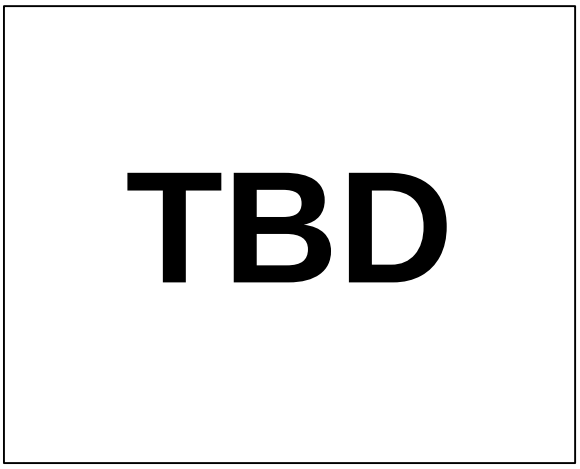


Figure 46. Transmit Spectrum, PA2 Output Power = 17 dBm, RF Frequency = 460 MHz, Data Rate = 7.2 kbps, Frequency Deviation = 2.0 kHz, Modulation = 2GFSK, BT = 0.5, V_{DD} = 3.0 V, T_A = 25°C

868 MHZ—RECEIVE

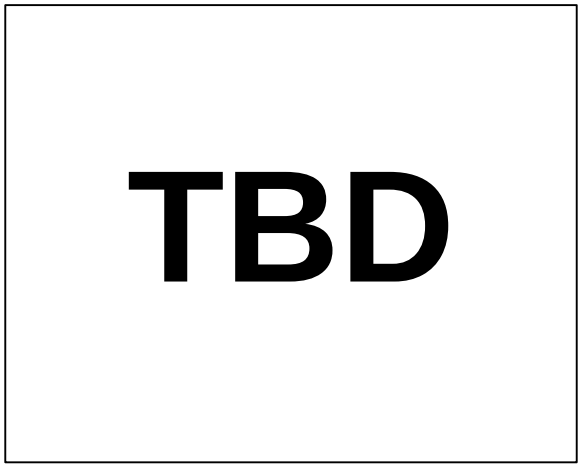


Figure 47. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 868MHz_4.8 kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

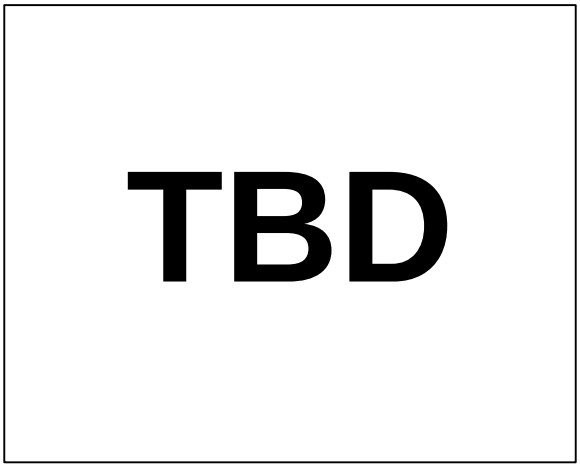


Figure 50. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}, Configuration 868MHz_100kbps, AFC Disabled

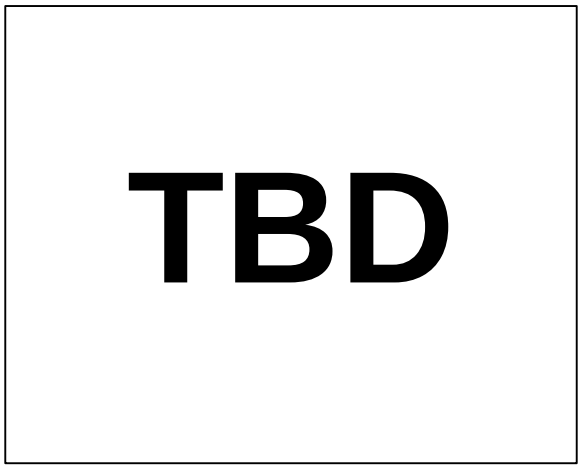


Figure 48. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 868MHz_100 kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

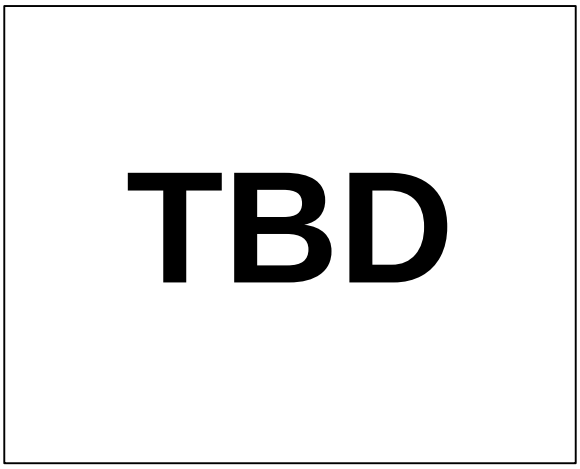


Figure 51. Receiver Close-In Blocking vs. Temperature and V_{DD}, Configuration 868MHz_4.8 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

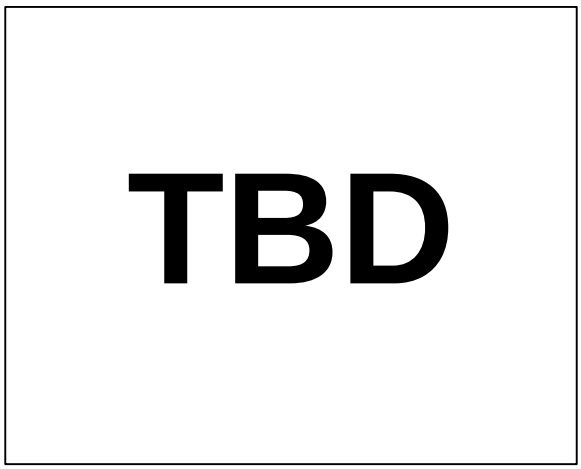


Figure 49. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}, Configuration 868MHz_4.8kbps, AFC Disabled

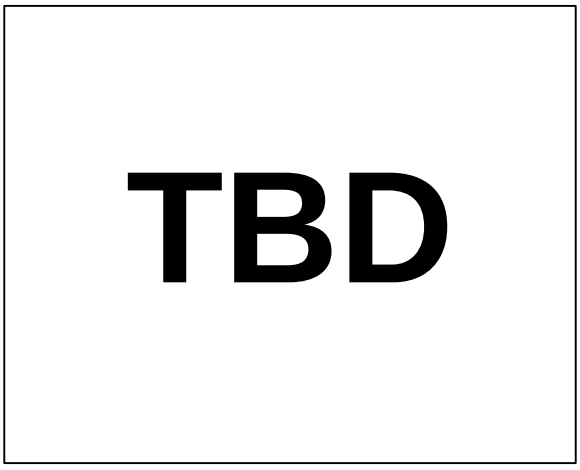


Figure 52. Receiver Close-In Blocking vs. Temperature and V_{DD}, Configuration 868MHz_100 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

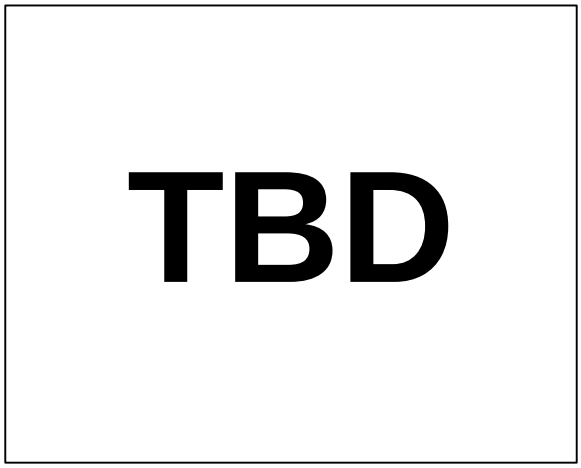


Figure 53. Receiver Wideband Blocking vs. Temperature and V_{DD}, Configuration 868MHz_4.8 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

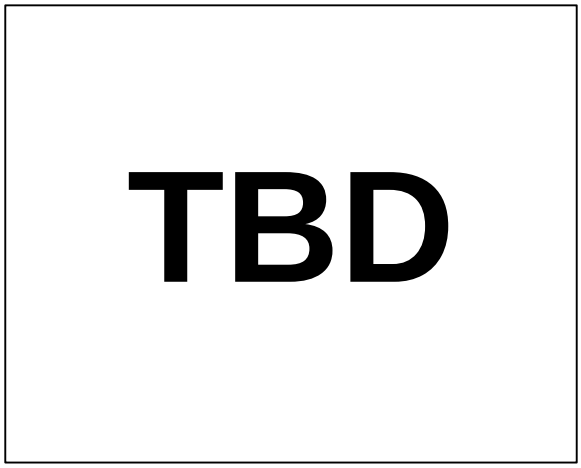


Figure 54. Receiver Wideband Blocking vs. Temperature and V_{DD}, Configuration 868MHz_100kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

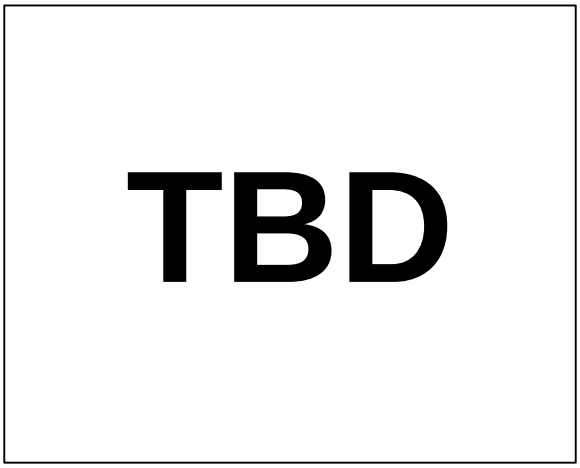


Figure 55. Packet RSSI Error vs. RF Input Power with One-Point Calibration at −70 dBm, Configuration 868MHz_4.8 kbps, V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

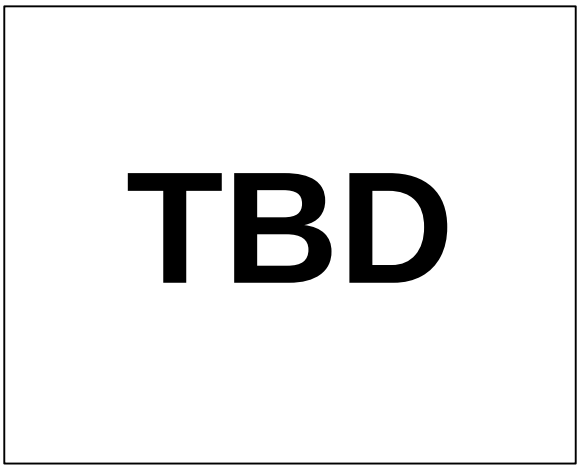


Figure 56. Packet RSSI Error vs. RF Input Power with One-Point Calibration at −70 dBm, Configuration 868MHz_100 kbps, V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

868 MHZ—TRANSMIT

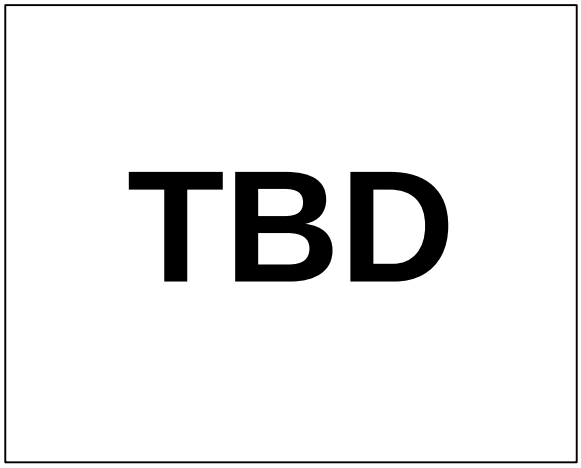


Figure 57. Phase Noise vs. Frequency Offset, RF Frequency = 868 MHz, PA2 Output Power = 17 dBm, V_{DD} = 3.0 V, T_A = 25°C

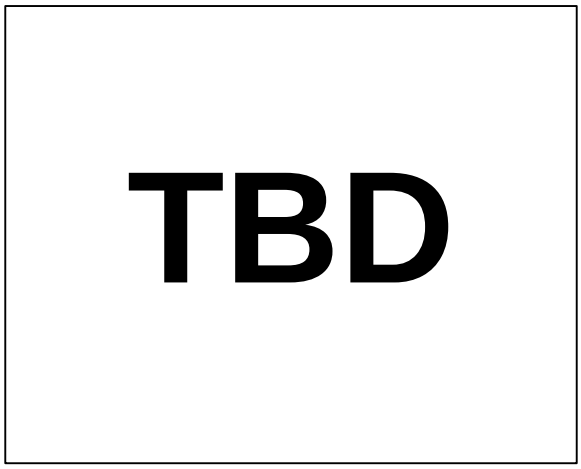


Figure 58. PA2 Output Power vs. PA_FINE Setting, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 868 MHz

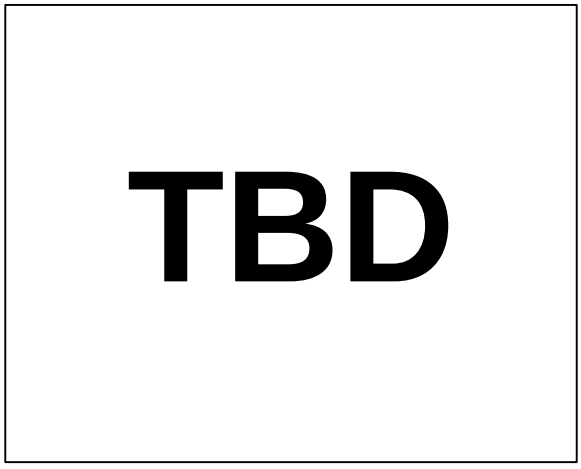


Figure 59. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 868 MHz

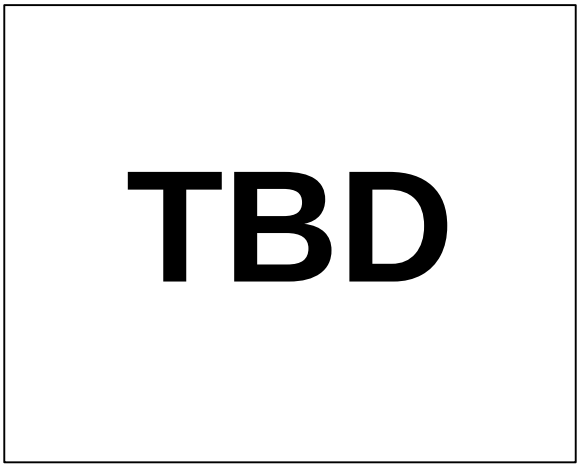


Figure 60. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, RF Frequency = 868 MHz, V_{DD} = 3.0 V, T_A = 25°C

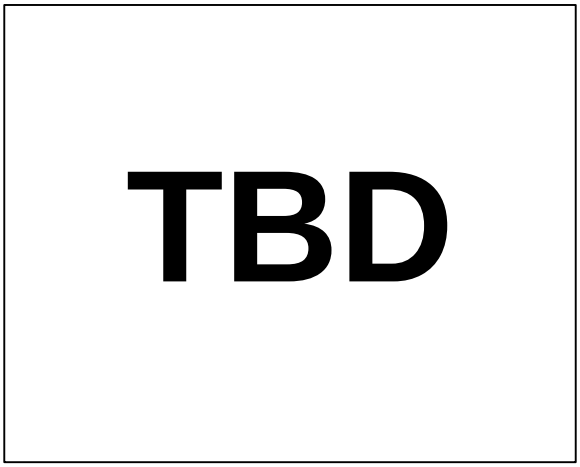


Figure 61. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 868 MHz, V_{DD} = 3.0 V, T_A = 25°C

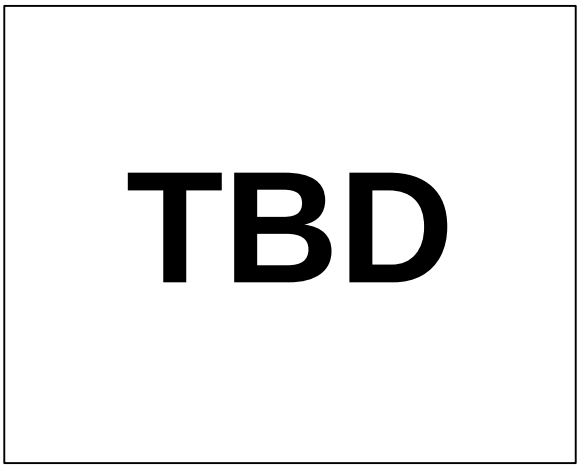


Figure 62. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 868 MHz, Data Rate = 4.8kbps, Frequency Deviation = 2.4 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

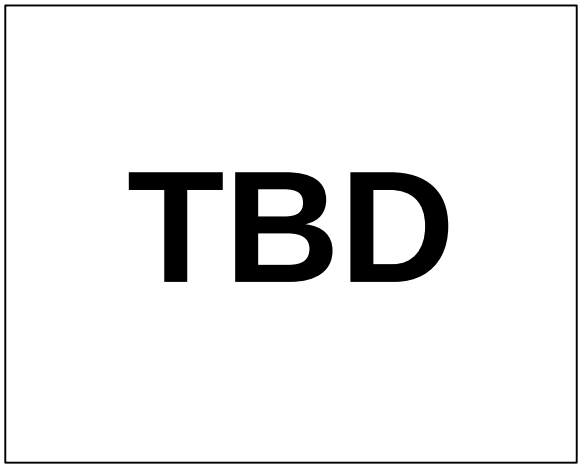


Figure 63. Transmit Spectrum, PA2 Output Power = 17 dBm, RF Frequency = 433 MHz, Data Rate = 4.8kbps, Frequency Deviation = 2.4 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

915 MHZ—RECEIVE

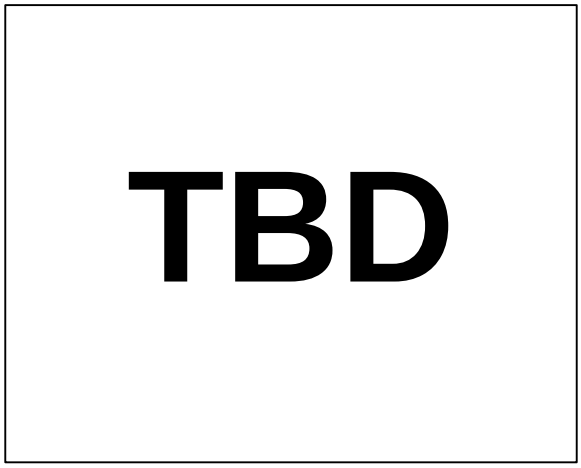


Figure 64. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 915MHz_50kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

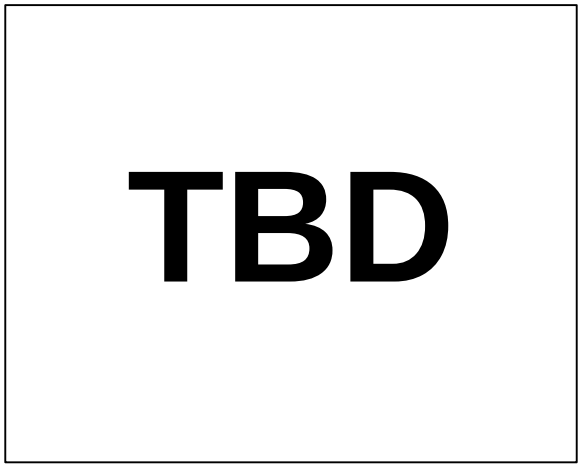


Figure 67. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}, Configuration 915MHz_150kbps, AFC Disabled

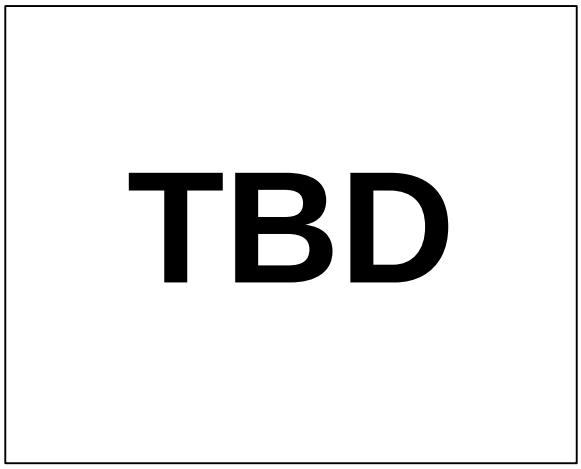


Figure 65. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 915MHz_150kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

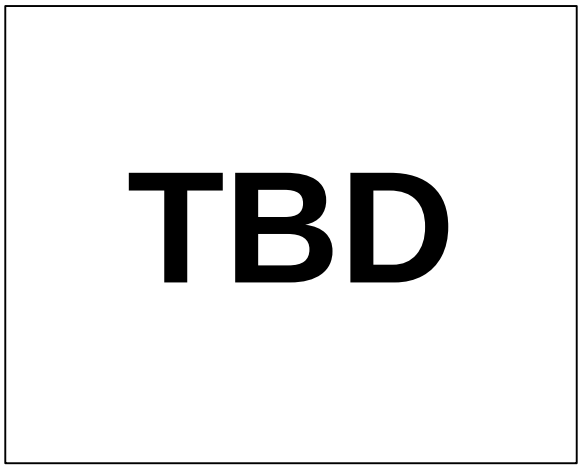


Figure 68. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}, Configuration 915MHz_300kbps, AFC Disabled

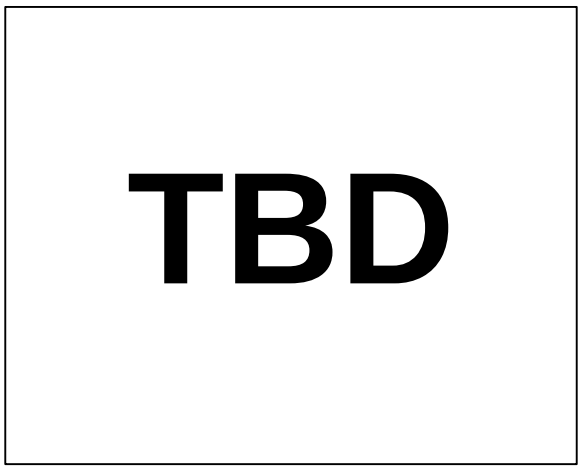


Figure 66. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 915MHz_300kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

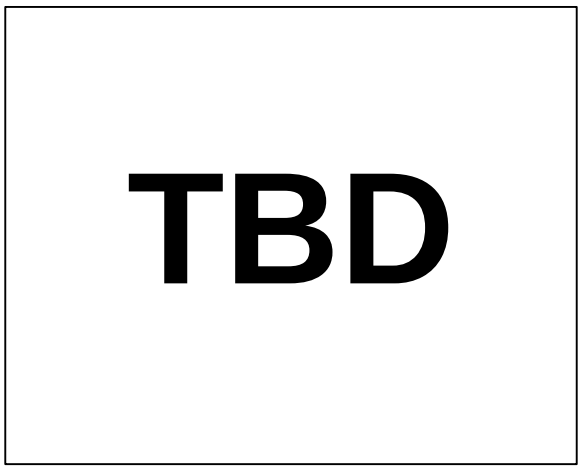


Figure 69. Receiver Close-In Blocking vs. Temperature and V_{DD}, Configuration 915MHz_150kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

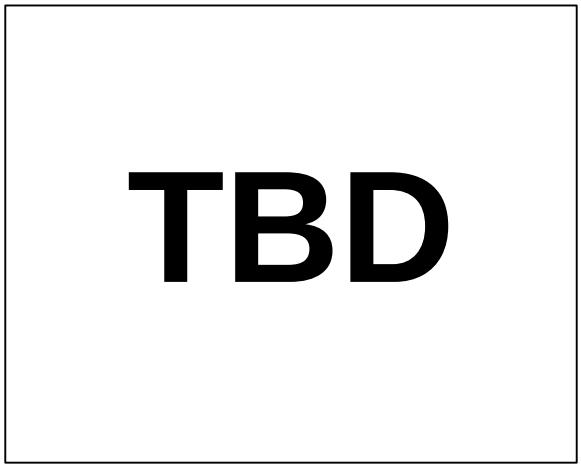


Figure 70. Receiver Close-In Blocking vs. Temperature and V_{DD}, Configuration 915MHz_300kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

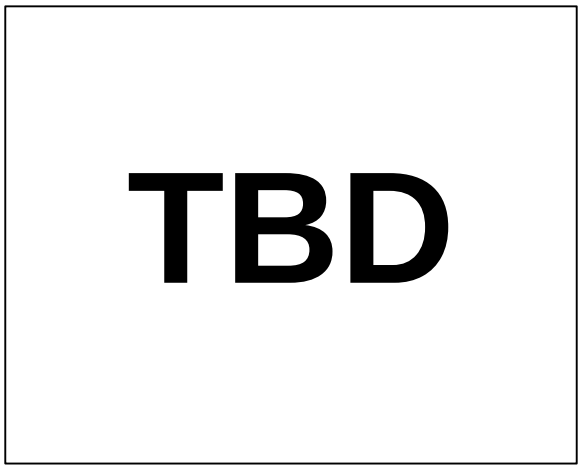


Figure 71. Receiver Wideband Blocking vs. Temperature and V_{DD}, Configuration 915MHz_150kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

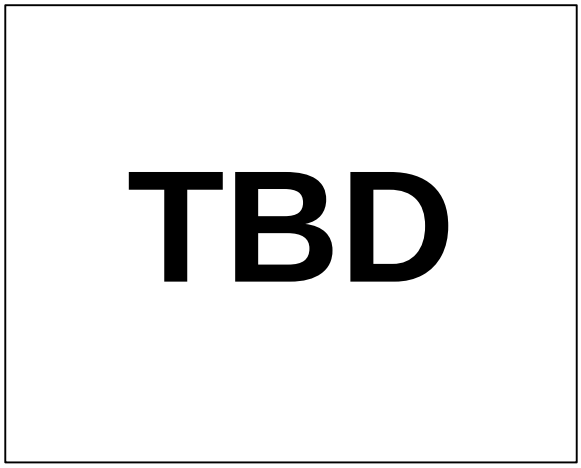


Figure 72. Receiver Wideband Blocking vs. Temperature and V_{DD}, Configuration 915MHz_300kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

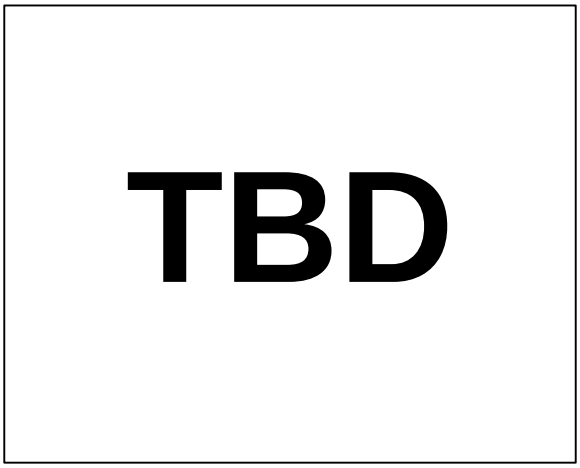


Figure 73. Packet RSSI Error vs. RF Input Power with One-Point Calibration at –70 dBm, Configuration 915MHz_150kbps, V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

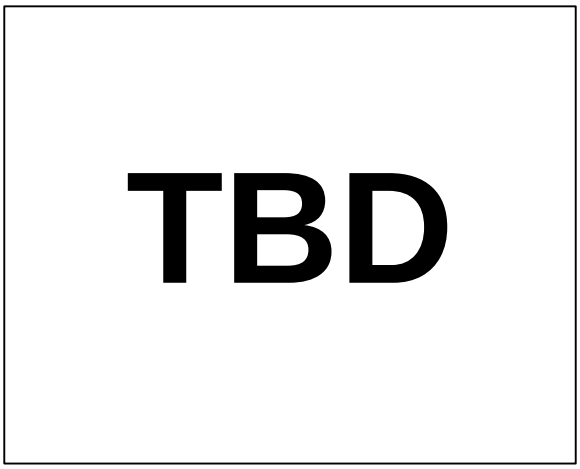


Figure 74. CCA RSSI Error vs. RF Input Power with One-Point Calibration at –70 dBm, Configuration 915MHz_150 kbps, V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

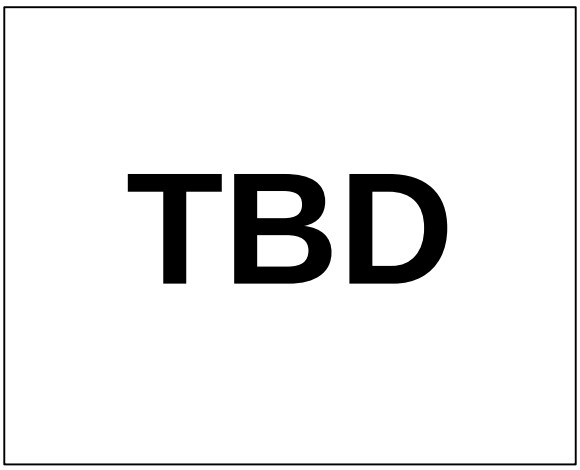


Figure 75. Packet RSSI Error vs. RF Frequency with One-Point Calibration at –80 dBm, RF input power = -80dBm, Configuration 915MHz_150kbps, V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

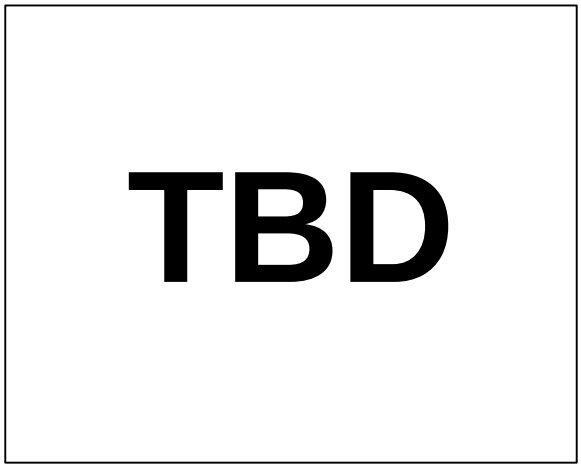


Figure 76. CCA RSSI Error vs. RF Frequency with One-Point Calibration at –80 dBm; RF Input Power = –80 dBm; Configuration: 915 MHz, 150 kbps; V_{DD} = 3.0 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

915 MHZ—TRANSMIT

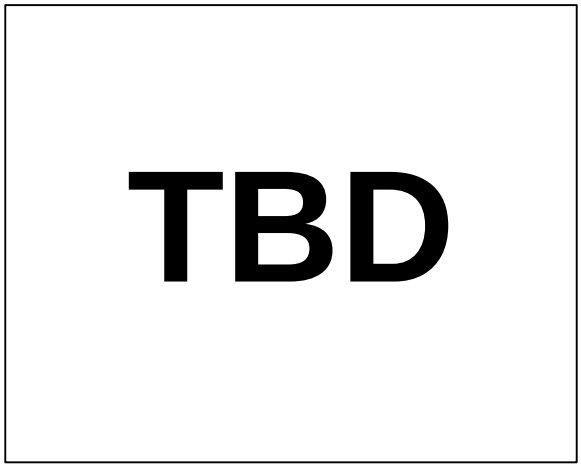


Figure 77. Phase Noise vs. Frequency Offset, RF Frequency = 915 MHz, PA2 Output Power = 17 dBm, V_{DD} = 3.0 V, T_A = 25°C

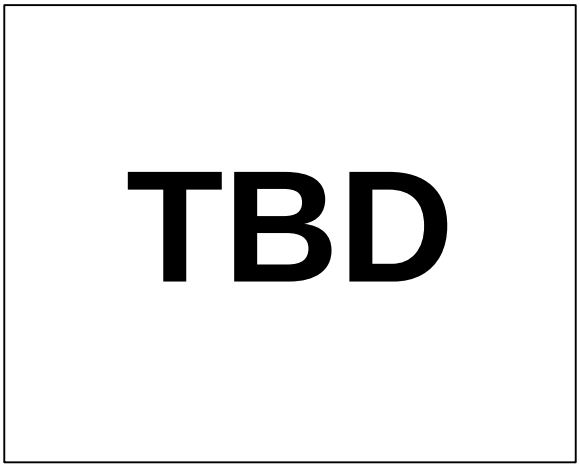


Figure 80. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, RF Frequency = 915 MHz, V_{DD} = 3.0 V, T_A = 25°C

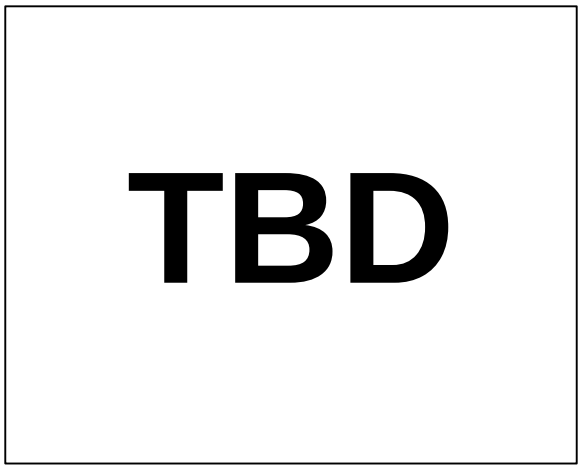


Figure 78. PA2 Output Power vs. PA_FINE Setting, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 915 MHz

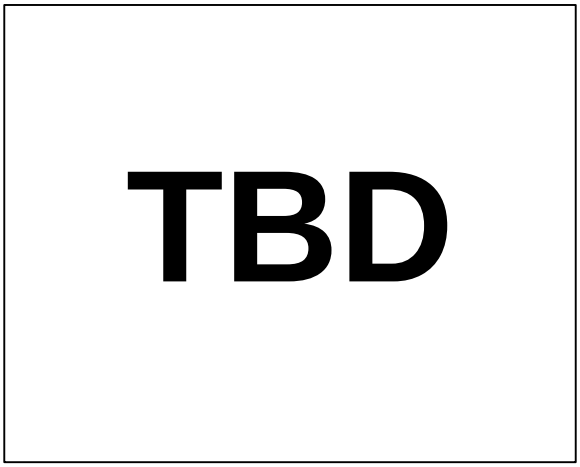


Figure 81. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 915 MHz, V_{DD} = 3.0 V, T_A = 25°C

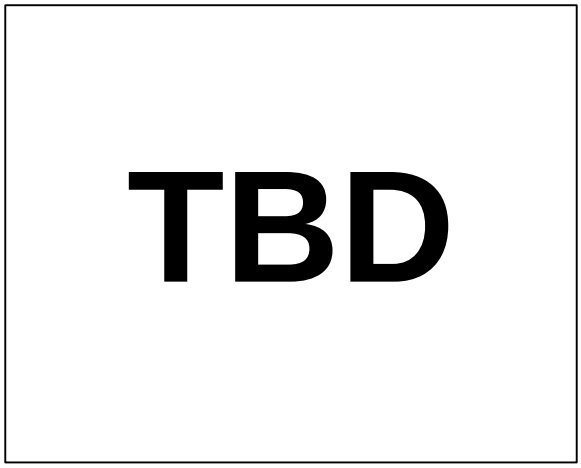


Figure 79. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 915 MHz

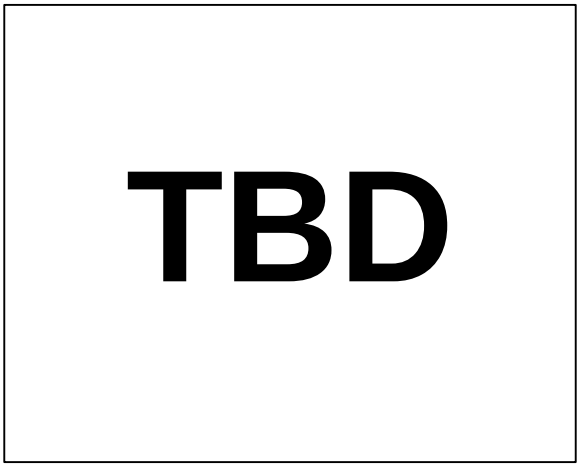


Figure 82. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 915MHz, Data Rate = 150 kbps, Frequency Deviation = 37.5 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

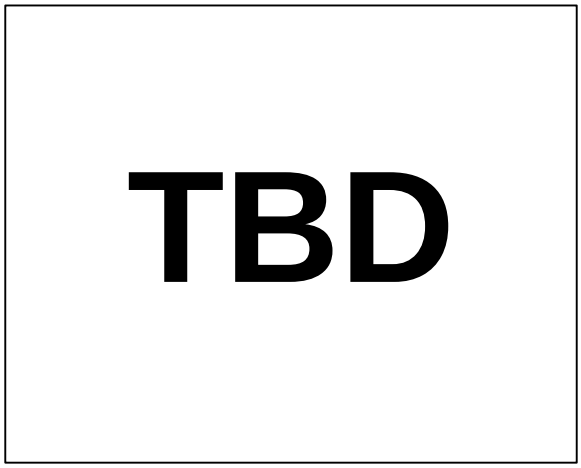


Figure 83. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 915MHz, Data Rate = 300 kbps, Frequency Deviation = 120 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

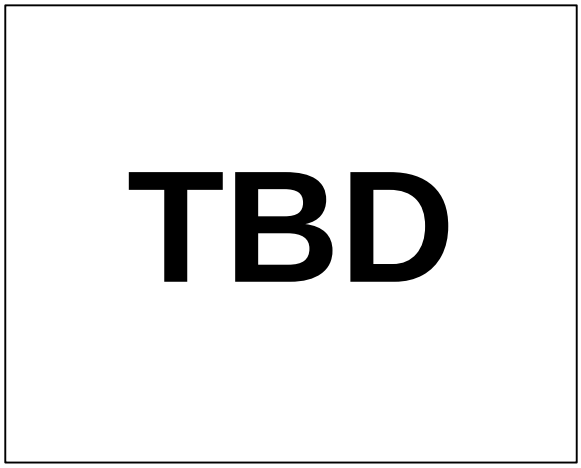


Figure 84. Transmit Eye Diagram, PA2 Output Power = 17 dBm, RF Frequency = 915MHz, Data Rate = 400 kbps, Frequency Deviation = 120 kHz, Modulation = 4GFSK, V_{DD} = 3.0 V, T_A = 25°C

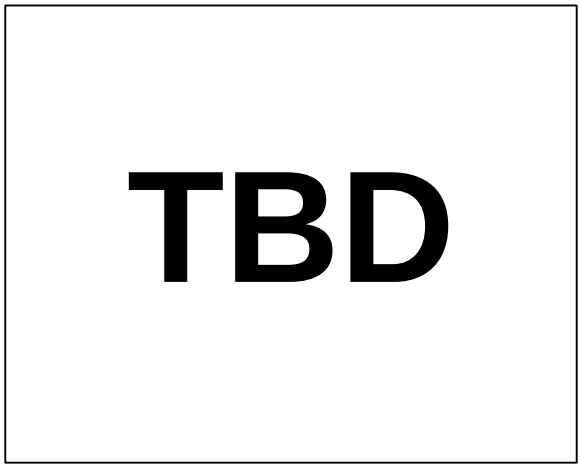


Figure 85. Transmit Spectrum, PA2 Output Power = 17 dBm, RF Frequency = 915 MHz, Data Rate = 300 kbps, Frequency Deviation = 120 kHz, Modulation = 2GFSK, V_{DD} = 3.0 V, T_A = 25°C

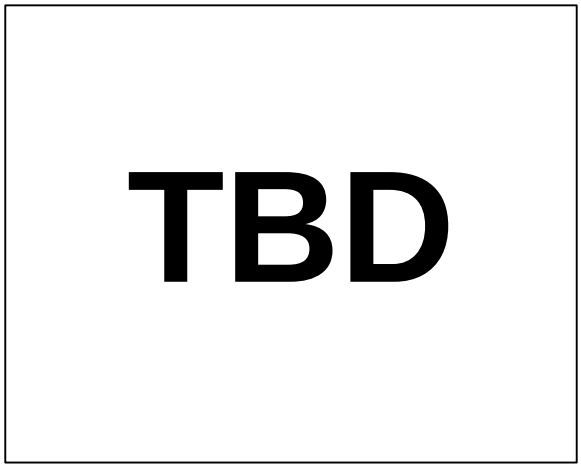


Figure 86. Transmit Spectrum, PA2 Output Power = 17 dBm, RF Frequency = 915 MHz, Data Rate = 400 kbps, Frequency Deviation = 66 kHz, Modulation = 4GFSK, V_{DD} = 3.0 V, T_A = 25°C

THEORY OF OPERATION

STATE MACHINE

TheADF7030-1 operates as a simple state machine as illustrated in Figure 87. The host processor can transition the ADF7030-1 between states by issuing single-byte commands over the SPI interface.

The ADF7030-1 processor handles the sequencing of various radio circuits and critical timing functions, thereby simplifying radio operation and easing the burden on the host processor.

The ADF7030-1 states are described in Table 24.

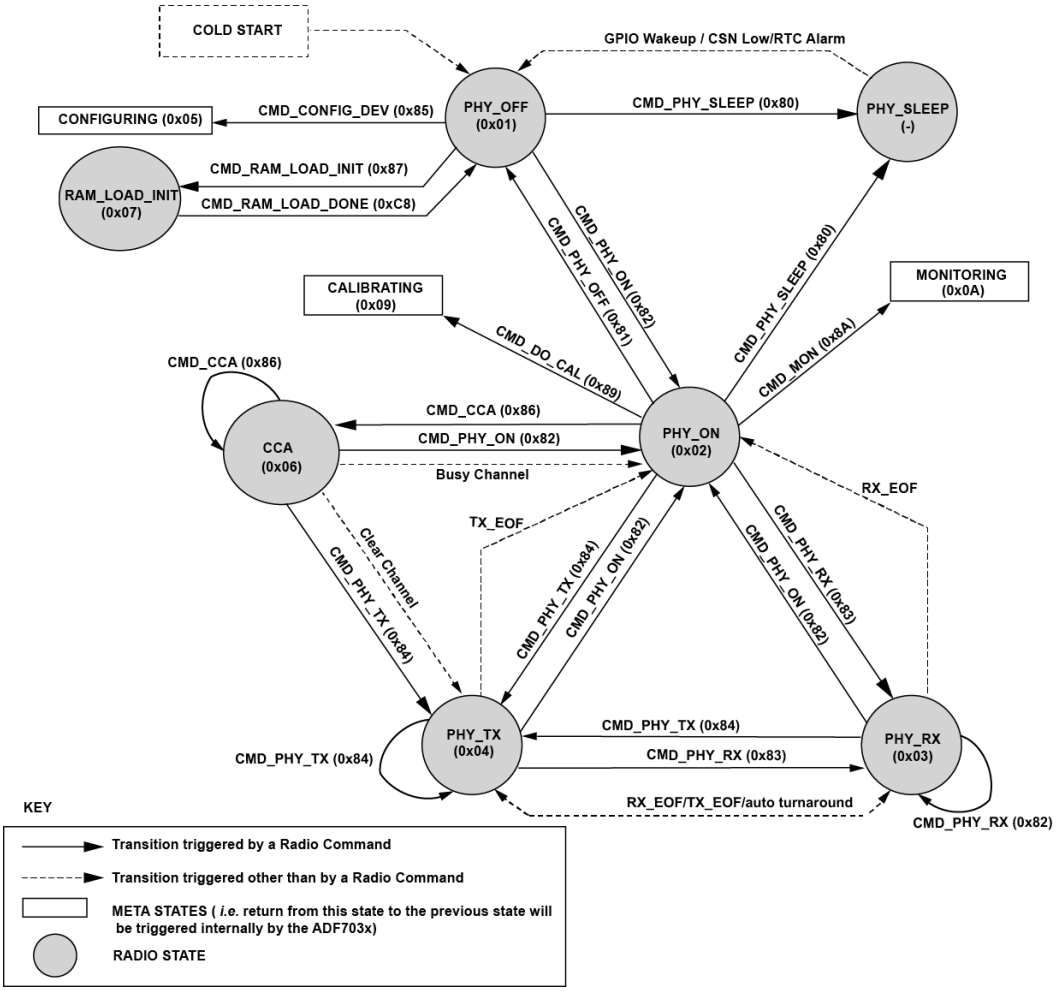


Figure 87. Radio State Machine Diagram

Table 24. Radio States

State	Description	Typical Current
PHY_SLEEP	In this state, the ADF7030-1 is in sleep. Memory can be optionally retained.	10 nA
PHY_OFF	In this state, the ADF7030-1 executes using its own internal oscillator clock. The host configures the radio from this state.	4 mA
PHY_ON	In this state, the external reference clock source is enabled. After entering this state, the ADF7030-1 is ready for the transmission and reception of packets.	4 mA
PHY_RX	In this state, the ADF7030-1 can receive and process an incoming packet.	22 mA to 27 mA
PHY_TX	In this state, the ADF7030-1 transmits the programmed packet data.	TBD mA (13 dBm)
CCA	In this state, the ADF7030-1 performs clear channel assessment.	22 mA to 27 mA

RADIO TIMING

Table 25. Radio Timing Specifications

Present State	Next State	Command/Bit	Command Initiated By	Transition Time (µs), Typical	Condition
Not Applicable	PHY_OFF	Cold Start	Application of power	TBD	
PHY_SLEEP	PHY_OFF	Wake-up from PHY_SLEEP (WUC timeout)	Automatic	TBD	
PHY_SLEEP	PHY_OFF	Wake-up from PHY_SLEEP ($\overline{CS}$ low or GPIO timeout)	Host	TBD	
Any	PHY_SLEEP	CMD_HW_RESET	Host	TBD	
PHY_OFF	PHY_SLEEP	CMD_PHY_SLEEP	Host	TBD	
PHY_OFF	PHY_ON	CMD_PHY_ON	Host	TBD	
PHY_OFF	PHY_OFF	CMD_CONFIG_DEV	Host	TBD	
PHY_ON	PHY_SLEEP	CMD_PHY_SLEEP	Host	TBD	
PHY_ON	PHY_OFF	CMD_PHY_OFF	Host	TBD	
PHY_ON	PHY_ON	CMD_DO_CAL	Host	TBD	
PHY_ON	CCA	CMD_CCA	Host	TBD	
PHY_ON	PHY_ON	CMD_MON	Host	TBD	
PHY_ON	PHY_TX	CMD_PHY_TX	Host	TBD	
PHY_ON	PHY_RX	CMD_PHY_RX	Host	TBD	
CCA	PHY_ON	CMD_PHY_ON	Host	TBD	
CCA	PHY_ON	Channel busy	Automatic	TBD	
CCA	CCA	CMD_CCA	Host	TBD	
CCA	PHY_TX	Clear channel	Automatic	TBD	
CCA	PHY_TX	CMD_PHY_TX	Host	TBD	
PHY_TX	PHY_ON	CMD_PHY_ON	Host	TBD	
PHY_TX	PHY_ON	TX_EOF	Automatic	TBD	
PHY_TX	PHY_TX	CMD_PHY_TX	Host	TBD	
PHY_TX	PHY_RX	CMD_PHY_RX	Host	TBD	
PHY_TX	PHY_RX	Automatic turnaround	Automatic	TBD	
PHY_RX	PHY_ON	CMD_PHY_ON	Host	TBD	
PHY_RX	PHY_ON	RX_EOF	Automatic	TBD	
PHY_RX	PHY_RX	CMD_PHY_RX	Host	TBD	
PHY_RX	PHY_TX	Auto Turnaround	Automatic	TBD	
PHY_RX	PHY_TX	CMD_PHY_TX	Host		

HOST INTERFACE

Physical Interface

The ADF7030-1 provides a simple host interface (HIF) that consists of a 4-wire standard SPI, a hardware reset pin ($\overline{RST}$), GPIOs, and interrupts pins (IRQs). The ADF7030-1 always acts as a slave to the host processor. The host uses the SPI to read and write ADF7030-1 memory and registers, to issue commands, and track status of the state machine, and to wake up the ADF7030-1 from PHY_SLEEP.

Host Interface Protocol

The ADF7030-1 implements a very simple protocol over the SPI interface. Using this protocol, the host processor can perform a number of operations, as described in the Memory Access section, the Radio Commands section, and the Status Byte section.

Memory Access

The memory access commands allow the host processor to read from and write to the internal memory of the ADF7030-1. Typically, the host uses these commands to update the configuration of the ADF7030-1 and to write packets for transmission or read received packets.

Radio Commands

There are two types of radio commands: a state machine radio command and a special radio command. A state machine command triggers a change of radio state as described in Table 26. A special radio command generates specific actions, for example, perform a system reset or to disable interrupt requests (IRQs), as described in Table 27.

Table 26. State Machine Radio Commands

Command	Description
CMD_PHY_SLEEP	Performs a transition of the device into the PHY_SLEEP state
CMD_PHY_OFF	Performs a transition of the device into the PHY_OFF state
CMD_PHY_ON	Performs a transition of the device into the PHY_ON state
CMD_PHY_RX	Performs a transition of the device into the PHY_RX state
CMD_PHY_TX	Performs a transition of the device into the PHY_TX state
CMD_CONFIG_DEV	Configures the ADF7030-1 based on the radio profile
CMD_CCA	Performs a transition of the device into the CCA state
CMD_DO_CAL	Executes selected calibration routines. Requires the OffLineCalibrations firmware module.
CMD_MON	Measures and reports the ADF7030-1 temperature

Table 27. Special Radio Commands

Command	Description
CMD_SYSTEM_RESET	Performs a system reset of the ADF7030-1
CMD_IRQ1_DIS_IRQ0_DIS	Disables IRQ_IN0 and IRQ_IN1 in triggering preloaded radio commands
CMD_IRQ1_DIS_IRQ0_EN	Disables IRQ_IN1 and enables IRQ_IN0 in triggering preloaded radio commands
CMD_IRQ1_EN_IRQ0_DIS	Enables IRQ_IN1 and disables IRQ_IN0 in triggering preloaded radio commands
CMD_IRQ1_EN_IRQ0_EN	Enables IRQ_IN1 and IRQ_IN0 in triggering preloaded radio commands

Status Byte

The ADF7030-1 reports the status via a status byte. The ADF7030-1 returns this byte on the SPI MISO in response to a NOP (0xFF) on the SPI MOSI.

Table 28. Status Byte Description

Bit	Name	Description
7	Reserved	Unused
6	Reserved	Unused
5	CMD_READY	0: the radio controller is not ready to receive a radio controller command 1: the radio controller is ready to receive a radio controller command
4	Reserved	Unused
3	ERR	0: no error 1: error (for example, unsupported destination state or internal error)
[2:1]	TRANSITION_STATUS	0: transition in progress 1: executing in a state 2: idle in a state
0	Reserved	Unused

RECEIVER

The ADF7030-1 features a fully integrated, highly configurable receiver that enables exceptionally high performance reception of narrow-band and wideband 2FSK/2GFSK signals. The receiver is based on a low IF architecture. Figure 88 shows a simplified block diagram of the receiver.

RF Front End

The receive signal is amplified by a differential LNA. The automatic gain control (AGC) circuit automatically controls the gain of the LNA. The LNA is followed by a quadrature downconversion mixer that converts the RF signal to the IF frequency. The fully integrated, fractional N frequency synthesizer generates the LO for the mixer. When the ADF7030-1 enters the PHY_RX state, the bandwidth of the LO is set automatically to ensure optimum interference rejection performance.

IF Processing

The quadrature IF signal is band-pass filtered using a high performance, configurable analog filter. The filter is followed by a programmable gain array (PGA) that is controlled by the AGC circuit.

The ADF7030-1 features a narrow-band and wideband IF processing path. In the narrow-band path, the IF signal is digitized by a high performance, high dynamic range ADC. RSSI, decimation, and offset correction are performed before the digitized IF is filtered using a configurable narrow-band digital channel filter.

In the wideband path, a limiter converts the IF signal to digital levels for the demodulator. The limiter also provides offset correction and RSSI, which is digitized using the ADC.

Table 29 lists the supported channel bandwidths and IF frequencies. The ADF7030-1 graphic user interface (GUI) automatically chooses the correct receive path, channel bandwidth, and IF frequency based on the data rate and modulation settings.

Table 29. Supported Channel Bandwidths and IFs

Narrowband Receive Path		Wideband Receive Path	
Channel BW (kHz)	IF (kHz)	Channel BW (kHz)	IF (kHz)
3.0	81.25	77.4	155
3.2	81.25	82.6	110
3.42	81.25	92	184
3.65	81.25	101.6	135
3.9	81.25	110.8	222
4.16	81.25	121.9	162
4.44	81.25	135.4	271
4.74	81.25	147.7	196
5.06	81.25	162.5	325
5.40	81.25	180.6	240
5.77	81.25	203.1	406
6.16	81.25	221.6	295
6.57	81.25	243.7	487
7.02	81.25	270.8	360
7.5	81.25	304.7	609
8.05	81.25	325	432
8.54	81.25	375	750
9.12	81.25	406.25	540
9.74	81.25	443.18	886
10.4	81.25	487.5	648
11.1	81.25		
11.85	81.25		
12.65	81.25		
13.51	81.25		
14.42	81.25		
15.39	81.25		
16.44	81.25		
17.55	81.25		
18.73	81.25		
20.00	81.25		

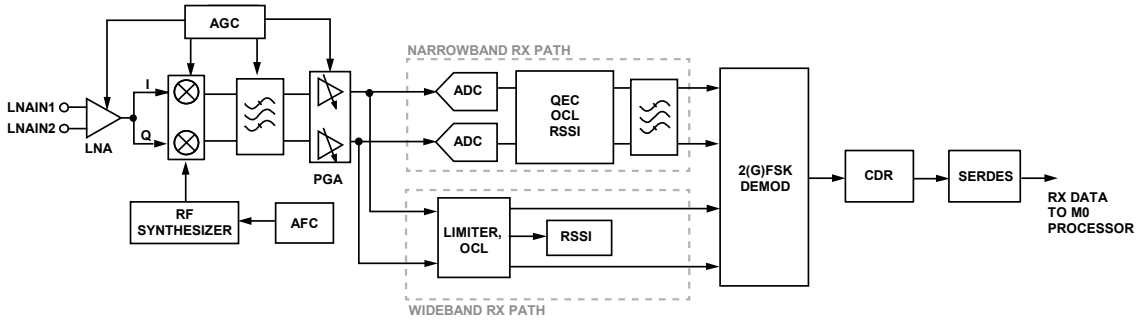


Figure 88. Receiver Block Diagram

AGC

AGC is enabled by default and keeps the receiver gain at the correct level by selecting the LNA, mixer, and filter gain settings based on the measured RSSI level.

AFC

The ADF7030-1 features an internal real-time automatic frequency control loop. In receive mode, the control loop automatically monitors the frequency error during the packet preamble sequence and adjusts the receiver synthesizer local oscillator. AFC is supported without the need for any additional preamble bits in the received packet.

Baseband Processing

The demodulator is based on a digital frequency correlator that performs filtering and frequency discrimination of the 2FSK/2GFSK spectrum. Following the demodulator is an oversampled digital clock and data recovery (CDR) PLL that resynchronizes the received bit stream to a local clock in all modulation modes. A serializer/deserializer (SERDES) block processes the received bit stream and produces the byte sized data for the ARM Cortex-M0 processor. The SERDES has a number of packet detection features, including preamble detection, sync word detection, and CRC calculation.

The ARM Cortex-M0 processor performs all of the byte level packet processing and packet management.

Received Signal Strength Indicator (RSSI)

The ADF7030-1 support accurate measurement of the received signal strength. To achieve the data sheet specified accuracies a one-point factory calibration is required (see the radio calibration section). The ADF7030-1 measures the RSSI during packet reception and the value is stored in a register for access by the host processor. The RSSI measurement is also used during CCA, where the RSSI measurement is evaluated against a user set threshold. The RSSI is reported in dBm.

TRANSMITTER

The ADF7030-1 transmitter supports 2FSK/2GFSK, 4FSK/4GFSK, and OOK modulation. It comprises a high performance PLL synthesizer and power efficient dual PAs. A block diagram of the ADF7030-1 transmitter architecture is shown in Figure 89. All blocks are fully integrated.

Synthesizer and VCO

A fully integrated low noise PLL synthesizer and VCO generate both the transmit signal and the receiver LO signal.

The synthesizer loop filter is fully integrated on chip and has a programmable bandwidth. On entering the PHY_RX state, the ADF7030-1 sets a narrow bandwidth to ensure optimum receiver rejection. In the PHY_TX state, the bandwidth is chosen to ensure optimum modulation quality.

A high speed, fully automatic calibration scheme ensures that the frequency and amplitude characteristic of the VCO are maintained over temperature, supply voltage, and process variations. The calibration is automatically performed when the CMD_PHY_RX or CMD_PHY_TX command is issued.

Power Amplifiers

The ADF7030-1 has two integrated power amplifiers. PA1 and PA2 are designed for optimum power consumption performance at 13 dBm and 17 dBm, respectively. The PAs cannot be operated simultaneously. The user selects the appropriate PA for their specific system. The power amplifiers are designed as Class F.

For systems where very fine power control is required, a PA microsetting can be used to achieve 0.1 dB of resolution across the power range. To reduce spectral splatter when the PA is turning on and off, a programmable PA ramp is provided.

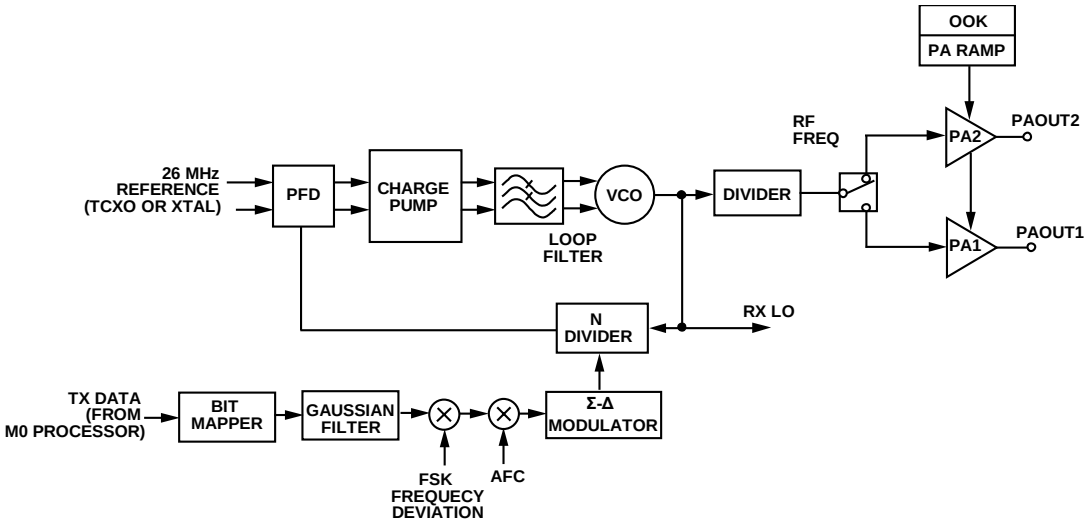


Figure 89. Transmitter Block Diagram

Transmit Modulation Schemes

The ADF7030-1 supports 2FSK/2GFSK and 4FSK/4GFSK modulation in transmit mode. In 2FSK/2GFSK mode, a binary zero value generates a –Fdev tone. A binary one generates a +Fdev tone. In 4FSK/4GFSK, the symbol mapping is configurable.

OOK modulation is also supported in transmit mode at a data rate of 16.384 kbps.

Transmit Filtering

The ADF7030-1 supports Gaussian filtering in both 2FSK and 4FSK mode. Gaussian filtering reduces the occupied bandwidth of the signal by digitally prefiltering the transmit data. The BT factors is configurable with the following options: 0.5, 0.4, 0.35, or 0.3. Reducing BT increases the roll-off factor of the filter resulting in a narrower signal bandwidth. As BT is reduced, intersymbol interference is introduced, which affects the receiver sensitivity performance.

RADIO CALIBRATION

To ensure that the ADF7030-1 radio performance meets the data sheet specifications, it is necessary to perform a calibration of the radio. To ease the processing burden on the host processor, the radio calibration routine is provided as a downloadable firmware module.

The calibration is fully autonomous when initiated by the CMD_DO_CAL command. On subsequent configurations of the ADF7030-1, the host processor can include the calibration settings in the configuration settings being written to the ADF7030-1.

Minimum Requirements

A one-time radio calibration, at room temperature, is the minimum requirement to ensure radio functionality. Calibration data is maintained in the PHY_SLEEP state if memory retention is enabled. If the memory is not retained, then the host processor must replay the calibration data to the ADF7030-1.

Requirements for Best Performance

It is recommended to complete a full calibration of the radio if the temperature changes by ±25°C from the temperature at which the previous calibration was executed. It is also recommended to complete a full calibration of the radio every 24 hours of operation.

PACKET HANDLING

The ADF7030-1 includes comprehensive transmit and receive packet management capabilities and can be configured for use with a wide variety of packet-based radio protocols.

IEEE 802.15.4g Packet Mode

The ADF7030-1 supports the multirate frequency shift keying (MR-FSK) PHY 802.15.4g specified packet format in the IEEE 802.15.4g-2012 standard with FEC, whitening and interleaving at data rates of up to 150 kbps.

Generic Packet Mode

The ADF7030-1 supports a wide variety of packet formats via its fully flexible generic packet format. In generic packet transmit mode, the ADF7030-1 can be configured to add preamble, sync word, and CRC to the payload data stored in the packet memory. The number of preamble bits and sync bits is programmable, and an optional length field can be added to allow packet length decoding at the receiver. The CRC polynomial and length are fully programmable in generic packet mode.

Transmitting and Receiving packets

The ADF7030-1 can be programmed to transmit and receive variable and fixed length payloads. The packet data to be transmitted must be written by the host into the ADF7030-1 internal memory. 511 bytes of dedicated RAM are available to store, transmit, and receive packets. For payload lengths greater than 511 bytes, the ADF7030-1 provides a rolling buffer mode.

To transmit or receive a packet, the host processor must first configure the ADF7030-1. Then, the host processor issues the commands to place the ADF7030-1 into the PHY_RX state or the PHY_TX state. After either state is entered, the ADF7030-1 automatically starts transmitting or receiving a packet.

In transmit mode, a preamble, sync word, and cyclic redundancy check (CRC) can be added by the ADF7030-1 to the payload data stored in the RAM. In receive mode, the ADF7030-1 can qualify received packets based on preamble detection, sync word detection, or CRC validation. On reception of a valid packet, the received payload data is loaded to packet memory.

The host can track the progress of the transmission or reception of a packet by monitoring the interrupt signals coming from the ADF7030-1. There are two independent logical interrupts from the ADF7030-1, and events can be configured to trigger one or both of these logical interrupts.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

A typical application circuit is shown in Figure 90. Refer to the ADF7030-1 Hardware Reference Manual for a comprehensive guide on application circuits, external hardware requirements, and RF matching for the ADF7030-1.

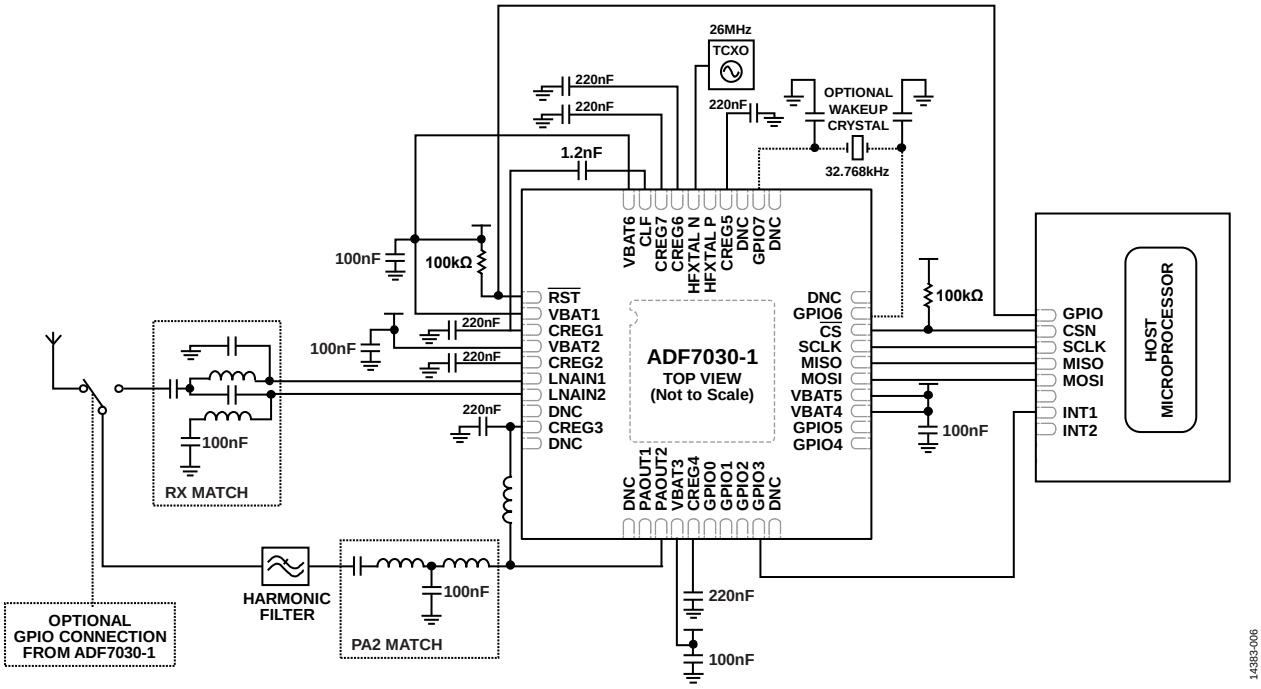


Figure 90. Typical Application Circuit with External Switch and TCXO Reference

SILICON ANOMALY

This anomaly list describes the known bugs, anomalies, and workarounds for the ADF7030-1.

Analog Devices, Inc., is committed, through future silicon revisions and/or firmware module revisions, to continuously improve functionality. Analog Devices tries to ensure that these future revisions of the ADF7030-1 silicon or firmware modules remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

The silicon revision information can be electronically determined by reading the PART_ID and ROM_ID fields from the ADF7030-1 memory locations described in Table 30.

Table 30. Silicon Revision ID

IF Field	Length (Bytes)	Memory Address
PART_ID	2	0x00007FF6
ROM_ID	1	0x00007FF9

ADF7030-1 FUNCTIONALITY ISSUES

Silicon Revision ID	Chip Marking	Silicon Status	Anomaly Sheet Revision	No. of Reported Anomalies
PART_ID = 0x0602 ROM_ID = 0x02	ADF7030-1BCPZN-U1 ADF7030-1BSTZN-U1	Prerelease	PrA	5

FUNCTIONALITY ISSUES

Table 31. Extra Bit Preceding Packet Preamble on Successive Transmit Packets [er001]

Background	A preamble sequence with the length controlled by GENERIC_PKT_FRAME_CFG0.PREAMBLE_LEN is transmitted at the start of a packet.
Issue	The first transmit packet has the correct preamble sequence and length. Subsequent packets prepend an extra random bit, before the preamble sequence.
Workaround	Issue a CMD_SYSTEM_RESET (0xC7) command and follow subsequent procedure as outlined in the ADF7030 Interface Programming Guide between successive packet transmissions.
Related Issues	PA ramp splatter for successive transmitter (Tx) packets [er002]

Table 32. PA Splatter After Completion of PA Ramp-Up on Successive Transmit Packets [er002]

Background	The ADF7030 uses a PA ramp profile to minimize spurious emissions and spectral leakage to adjacent channels while the PA is being switched on and off.
Issue	The first packet to be transmitted follows the correct PA ramp trajectory. Subsequent packets exhibit a small, spurious output coincident with the PA ramp completing.
Workaround	
Related Issues	None

Table 33. 1 mA Excess Current Consumption When Returning to PHY_ON State from PHY_TX [er003]

Background	The ADF7030 radio controller manages the power domains of several internal circuit blocks when transitioning between radio states.
Issue	Some Tx circuitry is not fully powered down after exiting the PHY_TX state (to the PHY_ON state), resulting in <1 mA excess power consumption in PHY_ON.
Workaround	
Related Issues	None.

Table 34. Rolling Buffer Interrupts Not Enabled [er004]

Background	The ADF7030 supports rolling buffer mode in transmit for long packets.
Issue	The lower half buffer free and upper half buffer free interrupts do not appear on GPIO3 and GPIO5 by default in transmit rolling buffer mode.
Workaround	
Related Issues	None.

Table 35. Custom CRC with Nonzero Seed Value [er005]

Background	The ADF7030 supports a custom cyclic redundancy check (CRC) with a programmable CRC polynomial and CRC seed.
Issue	The transmitted CRC is incorrect when using a custom CRC with a nonzero CRC seed value (GENERIC_PKT_CRC_SEED ≠ 0x000).
Workaround	When using a custom CRC, only use a CRC seed value of zero (GENERIC_PKT_CRC_SEED = 0x000).
Related Issues	None.

SECTION 1. ADF7030-1 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	Extra bit preceding packet preamble on successive transmit packets	Open
er002	PA splatter after completion of PA ramp-up on successive transmit packets	Open
er003	1 mA excess current consumption when returning to PHY_ON state from PHY_TX	Open
er004	Rolling buffer interrupts not enabled	Open
er005	Custom CRC with nonzero seed value	Open

DEVELOPMENT SUPPORT

DESIGN PACKAGE

This is a complete documentation and resource package for the ADF7030-1. It is recommended to download this package as a starting point for evaluation and development. It contains manuals, application notes, hardware information, and firmware modules.

REFERENCE MANUALS

ADF7030-1 Software Reference Manual (UG-1002)

The ADF7030-1 software reference manual is the detailed programming guide for the device. The ADF7030-1 hardware reference manual provides a description of the ADF7030-1 hardware features and application circuit requirements.

ADF7030-1 Hardware Reference Manual (UG-957)

The ADF7030-1 hardware reference manual provides a description of the ADF7030-1 radio functionality, hardware features, and application circuit requirements. It is intended as a resource for a hardware engineer designing a printed circuit board (PCB) that includes the ADF7030-1.

HARDWARE

Evaluation and development kits are available that include the ADF7030-1 radio daughter boards and the ADuCM3029 EZ-KIT evaluation board as the host processor. These kits are listed in Table 36.

Table 36. ADF7030-1 Evaluation and Development Kits

Model	Frequency (MHz)
ADF70301-915EZKIT	902 to 928
ADF70301-868EZKIT	863 to 876
ADF70301-433EZKIT	433 to 434
ADF70301-169EZKIT	169

A selection of individual daughter boards are also available covering various frequency bands and matching topologies.

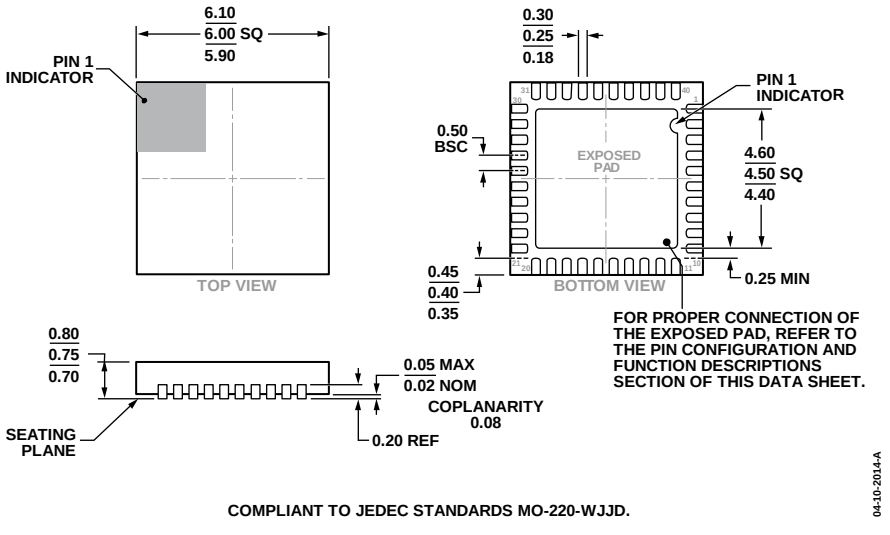
EVALUATION SOFTWARE

The EV-ADF70301-xxxEZKIT includes an easy to use evaluation and configuration GUI for the ADF7030-1. The GUI can be used for configuring the ADF7030-1, evaluating transmit and receive operation, and transmitting and receiving packets. This GUI allows the user to rapidly prototype different configurations with the ADF7030-1 and simplifies the migration to host code development.

EMBEDDED DEVELOPMENT

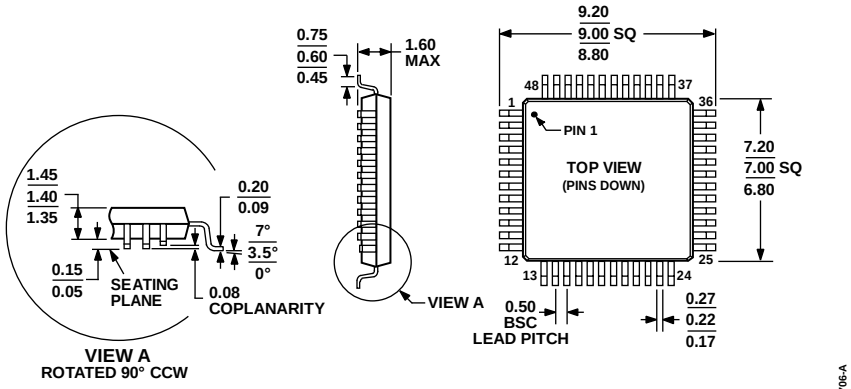
TBD

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 91. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 Package Height
(CP-40-17)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 92. 48-Lead Low Profile Quad Flat Package [LQFP]
7 mm × 7 mm Body,
(ST-48)
Dimensions shown in millimeters

PR14373-0-6/16(PrD)