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RF3183

QUAD-BAND/GSM850/EGSM900 /DCS/PCS/POWER AMPLIFIER MODULE

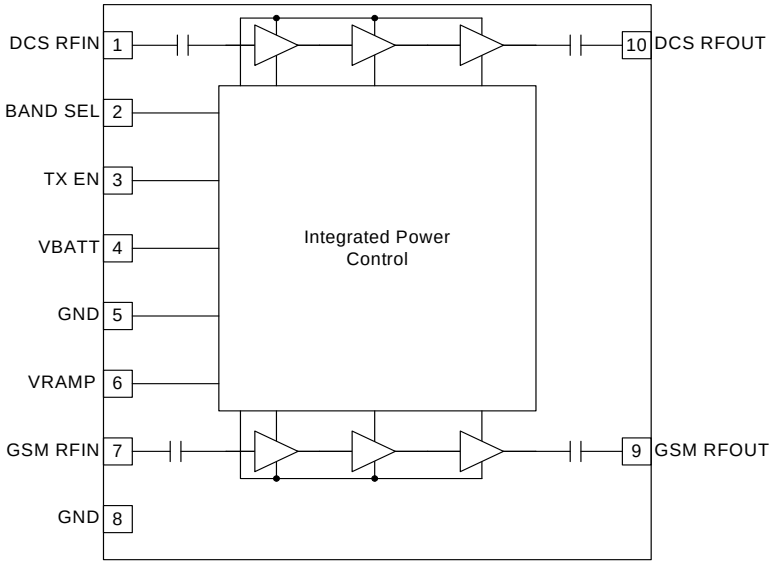
Package Style: Module (5mmx5mmx1mm)

Features

- Typical GMSK Efficiency GSM850/900 48/53% DCS/PCS 50/53%
- Auto V_{BATT} Tracking Circuit avoids Switching Transients at Low Supply Voltage
- Integrated Power Flattening Circuit Reduces Power and Current into Mismatch
- Integrated V_{RAMP} Rejection Filter Eliminates External Components

Applications

- Quad-Band GSM Handsets
- GSM Transmitter Line-ups
- Portable Battery-Powered Equipment
- GSM850/EGSM900/DCS/PCS Products
- GPRS Class 12 Compatible Products
- Mobile EDGE/GPRS Data Products



Functional Block Diagram

Product Description

The RF3183 is a high power amplifier module with integrated power control. The input and output terminals are internally matched to 50Ω. The amplifier devices are manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process. The module is designed to be the final amplification stage in a dual-mode GSM/EDGE mobile transmit lineup operating in the 824MHz to 915MHz (low) and 1710MHz to 1910MHz (high) bands (such as a cellular handset). Band selection is controlled by an input on the module which selects either the low or high band. The device is packaged on a 5mmx5mm laminate module with a protective plastic over-mold. The RF3183 features RFMD's latest integrated power flattening circuit, which significantly reduces current and power variation into load mismatch. The RF3183 provides excellent ESD protection at all the pins. The RF3183 also provides integrated V_{RAMP} rejection filter which improves noise performance and transient spectrum.

Ordering Information

RF3183	Quad-Band/GSM850/EGSM900 /DCS/PCS/Power Amplifier Module
	Power Amplifier Module, 5 Piece Sample Pack
RF3183PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{BATT})	-0.5 to +6.0	V
Power Control Voltage (V_{RAMP})	-0.5 to +3.0	V
Band Select	3.0	V
TX Enable	3.0	V
RF - Input Power	10.0	dBm
Max Duty Cycle	50	%
Output Load VSWR	10:1	
Operating Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
V_{RAMP}					
V_{RAMP} Input Current			40	µA	$V_{RAMP}=V_{RAMP,MAX}$
$V_{RAMP}=V_{RAMP, MAX}$			2.2	V	
$V_{RAMP}=V_{RAMP, MIN}$	0.25			V	
Band Select Switch					
BAND_SEL “HIGH”	1.5			V	High Band (DCS1800/PCS1900)
BAND_SEL “LOW”	0		0.7	V	Low Band (GSM850/EGSM900)
BAND_SEL Input Current	1		+10	uA	
TX_EN					
TX_EN “HIGH”	1.5			V	PA “ON”
TX_EN “LOW”	0		0.7	V	PA “OFF”
TX_EN Input Current	1		+10	uA	
Overall Power Supply					
V_{BATT} Range	3.0	3.6	4.5	V	
Off Current			10	uA	TX_EN Low
RF Impedance					
LB_RF IN		50		Ω	
LB_RF OUT		50		Ω	
HB_RF IN		50		Ω	
HB_RF OUT		50		Ω	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Cellular 850MHz Band GMSK Mode					Nominal test conditions unless otherwise stated. Temp=25 °C, V_{BATT}=3.6V, Freq=824MHz to 849MHz, 25% Duty Cycle, Pulse Width=1154µs, P_{IN}=-2dBm, BAND_SEL="Low", TX_EN="High", $V_{RAMP}=V_{RAMP,MAX}$
Operating Frequency Range	824		849	MHz	
Input Power Range, P_{IN}	-2	+1	+4	dBm	
Maximum Output Power 1	34.5	35.0		dBm	Temp=25 °C, V_{BATT}=3.6V
Maximum Output Power 2	32.5	33		dBm	Temp=85 °C, V_{BATT}=3.0V
Total Efficiency (PAE)	42	48		%	P_{IN}=+1dBm
Output Noise Power		-83	-82	dBm	869MHz to 894MHz, f_0=849MHz, $P_{OUT}\leq$Rated P_{OUT}, RBW=100kHz
Forward Isolation 1			-32	dBm	TX_EN=0V, VRAMP=$V_{RAMP,MIN}$, P_{IN}=+4dBm
Forward Isolation 2			-10	dBm	$V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
$2f_0$ Harmonics		-15	-10	dBm	$P_{OUT}\leq$Rated P_{OUT}
$3f_0$ Harmonics		-25	-15	dBm	$P_{OUT}\leq$Rated P_{OUT}
Fundamental Cross Band Coupling		-1	3	dBm	Measured at DCS_RF_{OUT} pin, $P_{OUT}\leq$Rated P_{OUT} at GSM_RFOUT pin
$2f_0$, $3f_0$ Cross Band Coupling		-22	-17	dBm	Measured at DCS_RF_{OUT} pin, $P_{OUT}\leq$Rated P_{OUT} at GSM_RFOUT pin
All Other Non-harmonic Spurious			-36	dBm	Over P_{IN} range, $P_{OUT}\leq$Rated P_{OUT}
Input VSWR		2:1	3:1		
Output Load VSWR Stability			-36	dBm	Load VSWR=5.1 All phase angles, Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=5:1, Full P_{IN} Range, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				Load VSWR=10:1, all phase angles. Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=10:1

Note: $V_{RAMP,MAX}$=2.2V, $V_{RAMP,MIN}$ =0.25V, Rated P_{OUT}=34.5dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM 900MHz Band GMSK Mode					Nominal test conditions unless otherwise stated. Temp=25 °C, V_{BATT}=3.6V, Freq=880MHz to 915MHz, 25% Duty Cycle, Pulse Width=1154µs, P_{IN}=-2dBm, BAND_SEL="Low", TX_EN="High", $V_{RAMP}=V_{RAMP,MAX}$
Operating Frequency Range	880		915	MHz	
Input Power Range, P_{IN}	-2	+1	+4	dBm	
Maximum Output Power 1	34.5	35		dBm	Temp=25 °C, V_{BATT}=3.6V
Maximum Output Power 2	32.5	33		dBm	Temp=+85°C, V_{BATT}=3.0V
Total Efficiency (PAE)	47	53		%	P_{IN}=+1dBm
Output Noise Power		-80	-79	dBm	925MHz to 935MHz, f_0=915MHz, $P_{OUT}\leq$Rated P_{OUT}, RBW=100kHz
		-83	-82	dBm	935MHz to 960MHz, f_0=915MHz, $P_{OUT}\leq$Rated P_{OUT}, RBW=100kHz
Forward Isolation 1			-32	dBm	TX_EN=0V, $V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
Forward Isolation 2			-10	dBm	$V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
$2f_0$ Harmonics		-15	-10	dBm	$P_{OUT}\leq$Rated P_{OUT}
$3f_0$ Harmonics		-25	-15	dBm	$P_{OUT}\leq$Rated P_{OUT}
Fundamental Cross Band Coupling		-1	3	dBm	Measured at DCS_RF_{OUT} pin, $P_{OUT}\leq$Rated P_{OUT} at GSM_RFOUT pin
$2f_0$, $3f_0$ Cross Band Coupling		-22	-17	dBm	Measured at DCS_RF_{OUT} pin, $P_{OUT}\leq$Rated P_{OUT} at GSM_RFOUT pin
All Other Non-harmonic Spurious			-36	dBm	Over P_{IN} range, $P_{OUT}\leq$Rated P_{OUT}
Input VSWR		2:1	3:1		
Output Load VSWR Stability			-36	dBm	Load VSWR=5:1 All phase angles. Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to 5:1 VSWR. Full P_{IN} Range, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				Load VSWR=10:1 All phase angles, Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=10:1

Note: $V_{RAMP,MAX}$=2.2V, $V_{RAMP,MIN}$=0.25V, Rated P_{OUT}=34.5dBm

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS 1800MHz Band GMSK Mode					Nominal test conditions unless otherwise stated. Temp=25 °C, V_{BATT}=3.6V, Freq=1710MHz to 1785MHz, 25% Duty Cycle, Pulse Width=1154µs, P_{IN}=-2dBm, BAND_SEL="High", TX_EN="High", $V_{RAMP}=V_{RAMP,MAX}$
Operating Frequency Range	1710		1785	MHz	
Input Power Range, P_{IN}	-2	+1	+4	dBm	
Maximum Output Power 1	32.0	33		dBm	Temp=25 °C, V_{BATT}=3.6V
Maximum Output Power 2	30	31		dBm	Temp=+85°C, V_{BATT}=3.0V
Total Efficiency (PAE)	43	50		%	P_{IN}=+1dBm
Output Noise Power		-81	-77	dBm	1805MHz to 1880MHz, f_0=1785MHz, $P_{OUT}\leq$Rated P_{OUT}, RBW=100KHz
Forward Isolation 1			-32	dBm	TX_EN=0V, $V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
Forward Isolation 2			-10	dBm	$V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
$2f_0$ Harmonics		-20	-10	dBm	$P_{OUT}\leq$Rated P_{OUT}
$3f_0$ Harmonics		-25	-15	dBm	$P_{OUT}\leq$Rated P_{OUT}
All Other Non-harmonic Spurious			-36	dBm	Over P_{IN} range, $P_{OUT}\leq$Rated P_{OUT}
Input VSWR		2:1	3:1		
Output Load VSWR Stability			-36	dBm	Load VSWR=5:1 All phase angles, Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=5:1, Full P_{IN} Range, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				Load VSWR=10:1 All phase angles Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=10:1

Note: $V_{RAMP,MAX}$=2.2V, $V_{RAMP,MIN}$ =0.25V, Rated P_{OUT}=32.0dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PCS 1900MHz Band GMSK Mode					Nominal test conditions unless otherwise stated. Temp=25 °C, V_{BATT}=3.6V, Freq=1850MHz to 1910MHz, 25% Duty Cycle, Pulse Width=1154µs, P_{IN}=-2dBm, BAND_SEL="High", TX_EN="High", $V_{RAMP}=V_{RAMP,MAX}$
Operating Frequency Range	1850		1910	MHz	
Input Power Range, P_{IN}	-2	+1	+4	dBm	
Maximum Output Power 1	32.0	33		dBm	Temp=25 °C, V_{BATT}=3.6V
Maximum Output Power 2	30	31		dBm	Temp=+85°C, V_{BATT}=3.0V
Total Efficiency (PAE)	45	53		%	P_{IN}=+1dBm
Output Noise Power		-81	-77	dBm	1930MHz to 1990MHz, f_0=1910MHz, $P_{OUT}\leq$Rated P_{OUT}, RBW=100kHz
Forward Isolation 1			-32	dBm	TX_EN=0V, $V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
Forward Isolation 2			-10	dBm	$V_{RAMP}=V_{RAMP,MIN}$, P_{IN}=+4dBm
$2f_0$ Harmonics		-20	-10	dBm	$P_{OUT}\leq$Rated P_{OUT}
$3f_0$ Harmonics		-25	-15	dBm	$P_{OUT}\leq$Rated P_{OUT}
All Other Non-harmonic Spurious			-36	dBm	Over P_{IN} range, $P_{OUT}\leq$32dBm
Input VSWR		2:1	3:1		
Output Load VSWR Stability			-36	dBm	Load VSWR=5:1 All phase angles, Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=5:1, Full P_{IN} Range, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				Load VSWR=10:1 All phase angles, Set V_{RAMP} where $P_{OUT}\leq$Rated P_{OUT} into 50Ω load, then load switched to VSWR=10:1

Note: $V_{RAMP,MAX}$=2.2V, $V_{RAMP,MIN}$ =0.25V, Rated P_{OUT}=32.0dBm

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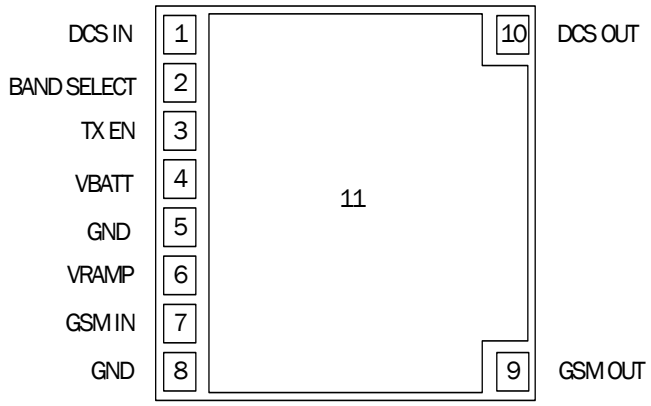
Pin	Function	Description
1	DCS_RFIN	RF input to the high-band PA. It is DC-blocked within the part.
2	BANDSEL	Digital input enables either the low band or high band amplifier die within the module. A logic low selects Low Band (GSM850/EGSM900), a logic high selects High Band (DCS1800/PCS1900). This pin is a high impedance CMOS input with no pull-up or pull-down resistors.
3	TX_EN	Digital input enables or disables the internal circuitry. When disabled, the module is in the OFF state, and draws virtually zero current. This pin is a high impedance CMOS input with no pull-up or pull-down resistors.
4	VBATT	Main DC power supply for all circuitry in the RF3183. Traces to this pin will have high current pulses during operation so proper decoupling and routing should be observed.
5	GND	Ground.
6	VRAMP	Analog signal used to control the output power. The signal also ramps the output power up and down. An internal 300kHz filter reduces switching ORFS resulting from transitions between DAC steps. Most systems will have no need for external V_{RAMP} filtering. This pin provides an impedance of approximately 60kΩ.
7	GSMIN	RF input to the low-band PA. It is DC-blocked within the part.
8	GND	Ground.
9	GSMOUT	RF output from the low-band PA. It is DC-blocked within the part.
10	DCSOUT	RF output from the high-band PA. It is DC-blocked within the part.
11	GND	Main ground pad in center of part. This pad should be tied to the main ground plane with as little loss as possible for optimum linearity.

Pin Out

Top View



Theory of Operation

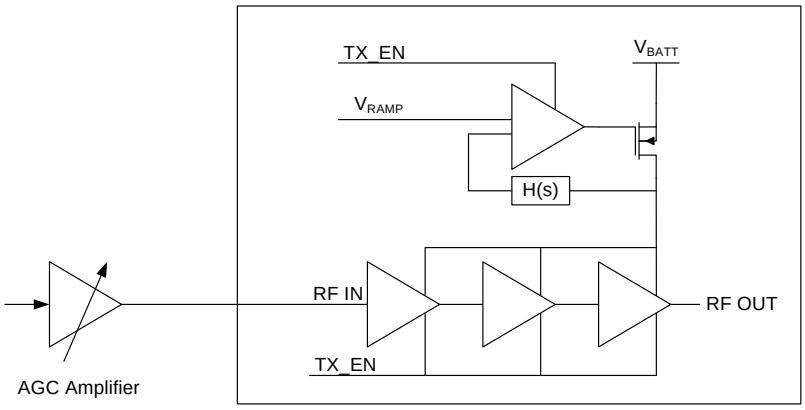


Figure 1. RF3183 Power Amplifier Simplified Block Diagram of a Single Band

Overview

The RF3183 is designed for use as the final RF amplifier in GSM850, EGSM900, DCS and PCS handheld digital cellular equipment, and other applications operating in the 824MHz to 915MHz, and 1710MHz to 1910MHz bands. The RF3183 is a high power, power amplifier module with PowerStar® integrated power control. The integrated power control circuitry provides reliable control of saturated power by a single analog voltage (V_{RAMP}). This control voltage can be driven directly from a DAC output. PowerStar®'s predictable power versus V_{RAMP} relationship allows single-point calibration in each band. Single-point calibration enables handset manufacturers to achieve simple and efficient phone calibration in production.

The RF3183 also features an integrated saturation detection circuit, which is an industry first for standard PA module products. The saturation detection circuit automatically monitors battery voltage, and adjusts the power control loop to reduce transient spectrum degradation that would otherwise occur at low battery voltage conditions. Prior to the implementation of the saturation detection circuit, handset designers were required to adjust the ramp voltage within the system software. RFMD's saturation detection circuit reduces handset design time and ensures robust performance over broad operating conditions.

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Power and Current Into Mismatch

Transmitters are often designed to operate only under perfect 50Ω loads. In the real application when a PA is subjected to mismatch conditions, performance degrades most likely in a reduction of output power, increased harmonic levels, increased transient spectrum, and catastrophic failures.

RF3183 has an integrated power flattening circuit that reduces the amount of current variation under load mismatch. When a mismatch is presented to the output of the PA, its output impedance is varied and could present a load that will increase output power. As the output power increases, so does current consumption. The current consumption can become very high if not monitored and limited. The power-flattening circuit is integrated onto the CMOS controller and requires no input from the user.

Into a mismatch, current varies as phase changes. The power-flattening circuit monitors current through an internal sense resistor. As current changes, the loop is adjusted in order to maintain current. Under nominal conditions, this loop is not activated and is seemingly transparent. The result is flatter power and reduced current into mismatch as shown in the following figures.

Test Condition: V_{BATT}=3.6V, RF_{IN}=1dBm, Temperature=25°C, Tx Frequency=915MHz

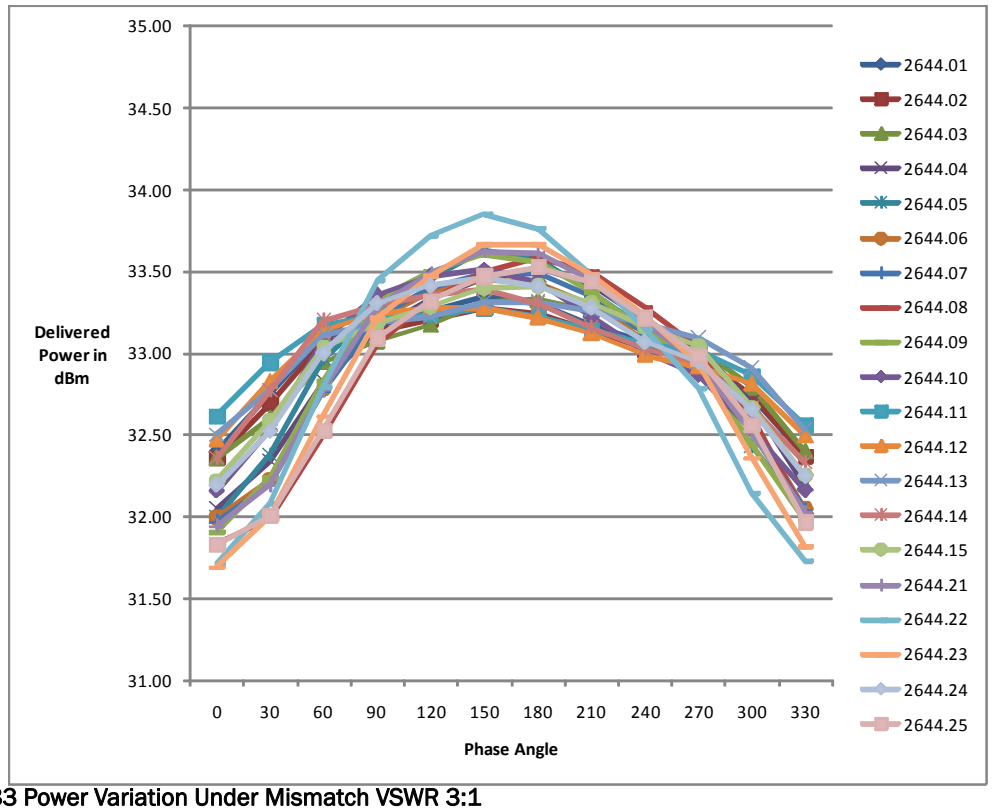

Figure 2. RF3183 Power Variation Under Mismatch VSWR 3:1

Test Condition: V_{BATT}=3.6V, RF_{IN}=1dBm, Temperature=25°C, Tx Frequency=915MHz

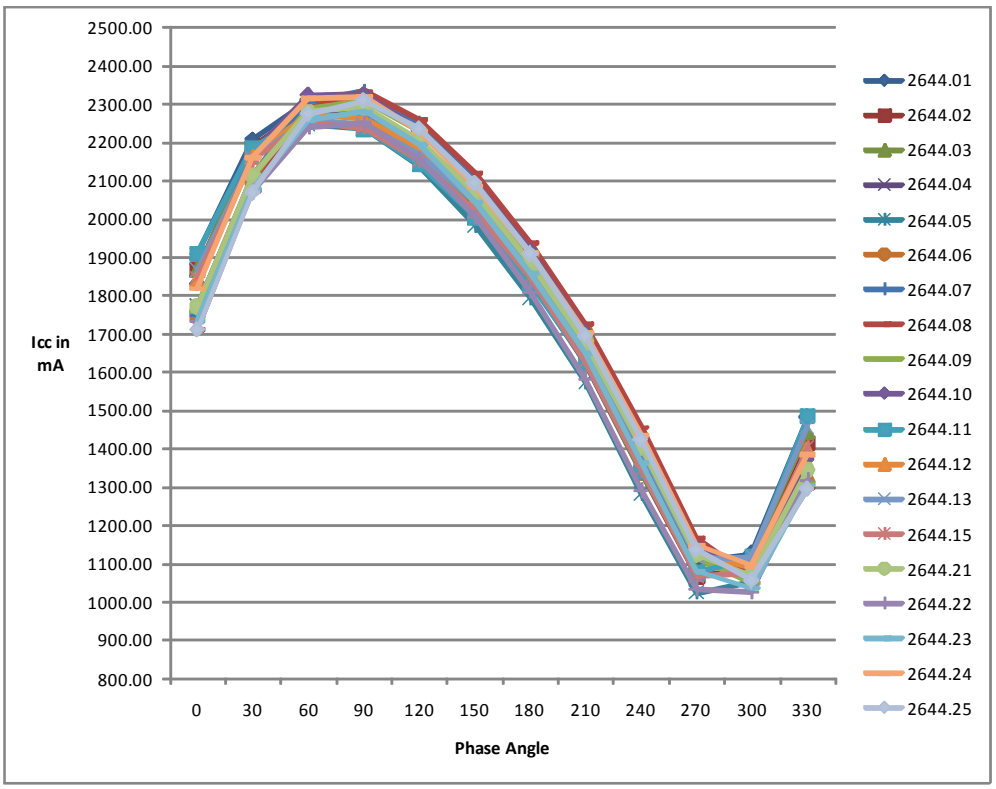

Figure 3. RF3183 Current Variation Under Mismatch VSWR 3:1

RF3183 operates as a traditional PowerStar® module. The incorporated control loop regulates the collector voltage of the amplifiers while the stages are held at a constant bias. The basic circuit diagram is shown in Figure 2.

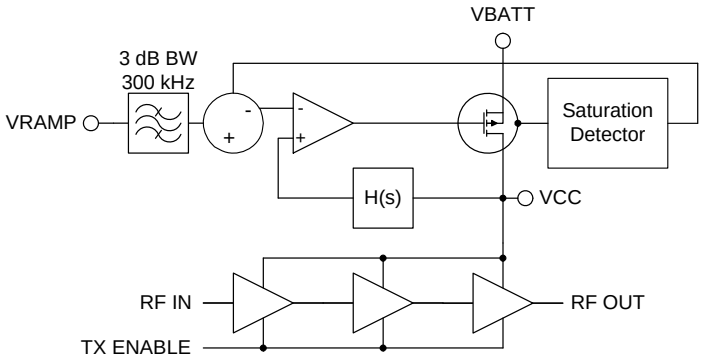

Figure 4. RF3183 Basic Circuit

By regulating the collector voltage (V_{CC}), the stages are held in saturation across all power levels. As V_{CC} is decreased, output power decreases as described by Equation 1. The equation shows that load impedance affects output power, but to a lesser degree than V_{CC} supply variations. Since the RF3183 regulates V_{CC}, the dominant cause of power variation is eliminated.

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$$P_{OUT_{dBm}} = 10\log\frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R1 \cdot 10^{-3}} \text{ (Eq. 1)}$$

RF3183 power is ramped up and down through the V_{RAMP} control voltage which in turn controls the collector voltage of the amplifier stages. The RF signal applied at the RF_{IN} pin must be a constant amplitude signal and should be high enough to saturate the amplifier in the GSM mode. The input power (P_{IN}) range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier and will increase the minimum output power of the RF3183.

The saturation detector circuit monitors the V_{BATT} and V_{CC} voltages and adjusts the power control loop to prevent the series-pass FET regulator from entering saturation. If the V_{CC} regulator were to saturate, the response time would increase dramatically. This is undesirable because the V_{CC} regulator must accurately follow the burst ramp up or ramp down applied to the V_{RAMP} pin, or the transient spectrum will degrade.

Power Ramping and Timing

The RF3183 should be powered on according to the Power-On Sequence provided in the datasheet. The power on sequence is designed to prevent operation of the amplifier under conditions that could cause damage to the device or erratic operation.

In the Power-On Sequence, there are some set-up times associated with the control signals of the RF3183. The most important of these is the settling time between TXEN going high and when V_{RAMP} can begin to increase. This time is often referred to as the "pedestal" and is required so that the internal power control loop and bias circuitry can settle after being turned on. The RF3183 requires at least 1.5µs or two quarter bit times for proper settling of the power control loop..

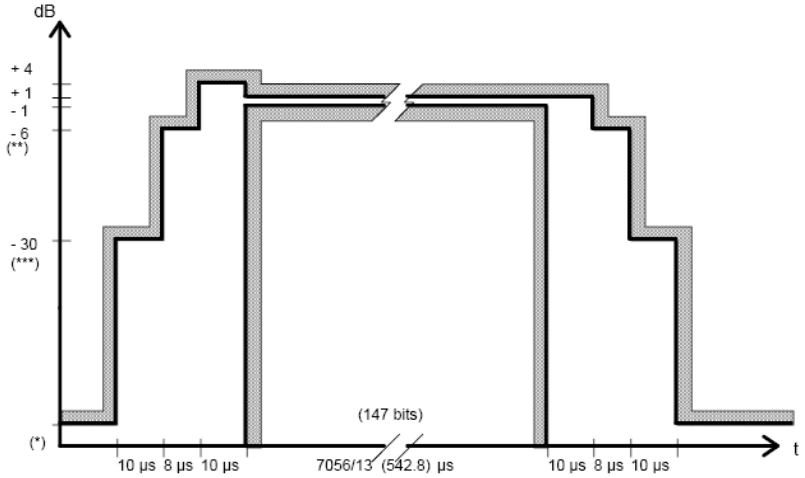

Figure 5. ETSI Time Mask for a Single GSM Time Slot

The V_{RAMP} waveform used with the RF3183 must be created such that the output power falls into this power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus V_{RAMP} response of the power amplifier. The PowerStar® control in the RF3183 is very capable of meeting switching transient requirements with the proper raised cosine waveform applied to the V_{RAMP} input. The ramping waveform on V_{RAMP} must not start until after TX_EN is asserted. A ramp of about 12us is required to control switching transients at high power levels.

The V_{RAMP} voltage range should be limited to min and max values in the specifications to avoid damage or undesirable operation. At some voltage below 0.3V, the CMOS controller switches off and turns off the PA. The effect of this is a discontinuity in the response curve. In order to guarantee minimum switching transients, it is recommended that the minimum ramp voltage be set slightly above the voltage where this discontinuity occurs (See Figure 3). The V_{RAMP} voltage at which the discontinuity occurs is unique to the design of the part and does not shift significantly across process. Figure 7 shows the power versus V_{RAMP} response curve for five parts which represent typical process variation of the discontinuity

Test Condition: 824MHz, 3.6V_{BATT}, 1dBm RFIN, 25°C Temp.

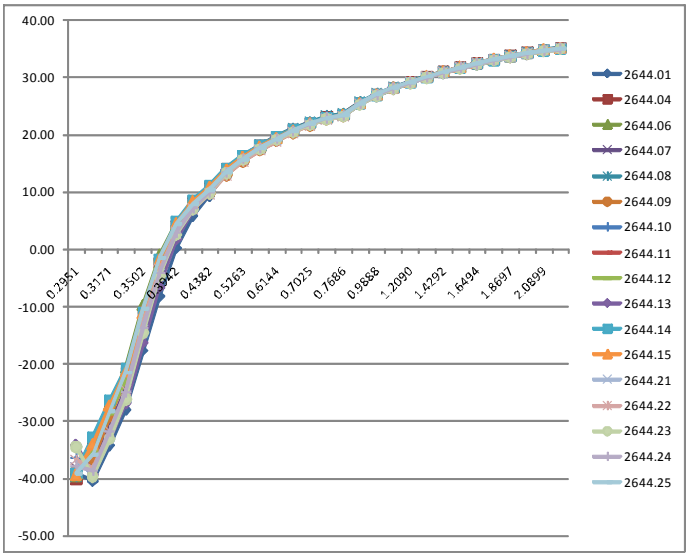

Figure 6. RF3183 LB P_{OUT} versus V_{RAMP}

As the V_{RAMP} voltage approaches its maximum, the linear regulator in the CMOS saturates, the output power reaches its maximum level, and the V_{RAMP} versus Output Power curve levels out. The saturation point of the linear regulator is directly proportional to the V_{BATT} supply voltage applied. The V_{RAMP} voltage can be increased above the saturation level, but the PA will not produce any higher output power. It is not recommended to apply a V_{RAMP} voltage above the absolute maximum specification, as the part could be damaged.

When the FET pass-device in the linear regulator saturates, the response time of the regulated voltage slows significantly. If the control voltage changes (as in ramp-down) the saturated linear regulator does not react fast enough to follow the ramp-down curve. The result is a discontinuity in the output power ramp and degraded switching transients. This usually occurs at low V_{BATT} levels where the regulated V_{CC} voltage is very near the supply voltage. The RF3183 incorporates a saturation detection circuit which senses if the FET pass-device is entering saturation and reduces V_{CC} to prevent it. This relieves the requirement of the transceiver controller to adjust the maximum V_{RAMP} when the battery voltage is low.

Design Considerations

There are several key factors to consider in the implementation of a mobile phone transmitter solution using the RF3183:

- System efficiency:

The RF output match can be designed to improve system efficiency by presenting a non 50Ω load. Output matching circuits for the RF3183 should be a compromise between system efficiency and power.

- Power variation due to supply voltage:

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Output power does not vary due to supply voltage under normal operating conditions. By regulating the collector voltage to the PA the voltage sensitivity is essentially eliminated. This covers most cases where the PA will be operated. However, as the battery discharges and V_{BATT} approaches its lower operating limit, the output power from the PA will start to drop. This cannot be avoided as a certain supply voltage is required to produce full output power. System specifications must allow for this power decrease.

Switching Transients due to low battery conditions are reduced by the saturation detection circuit in RF3183. The saturation detection circuit consists of a feedback loop which detects FET saturation. As the FET approaches saturation, the circuit adjusts the V_{CC} voltage in order to ensure minimum switching transients. The saturation detection circuit is integrated into the CMOS controller and requires no additional input from the user.

- Power variation due to temperature

RF3183 output power variation due to temperature is largest at low power levels and decreases at the upper power levels. This follows the ETSI specification limits which allow a larger tolerance over extreme conditions at low power levels. Since output power is controlled by an analog input, factors other than the power amplifier will have an effect on total system power variation. The entire system containing the RF3183 should be tested to determine whether compensation is necessary. At high temperatures and low battery voltages, the PA cannot support as high of an output power. In this condition, increasing V_{RAMP} will not provide more output power, so compensation may not provide the intended result.

- Noise Power

The bias point of the RF3183 is kept constant and the gain in the first stage is always high. This has the effect of maintaining a consistent noise power which does not increase at reduced output power levels. For that reason, noise power is at its highest when V_{RAMP} is at its maximum. The RF3183 does not create enough noise in the receive band to cause system receive band noise power failures, but it may amplify noise from other sources. Care must be taken to prevent noise from entering the power amplifier.

- Loop Stability and Loop Bandwidth variation across power levels

The design of a proper power control loop involves trade-offs affecting stability, transient spectrum and burst timing. In non-PowerStar® architectures, backing off power causes gain variation which can affect loop bandwidth. In RF3183 the loop bandwidth is determined by V_{CC} regulator bandwidth and does not change over output power. Loop stability is maintained since amplifier bias voltage is constant.

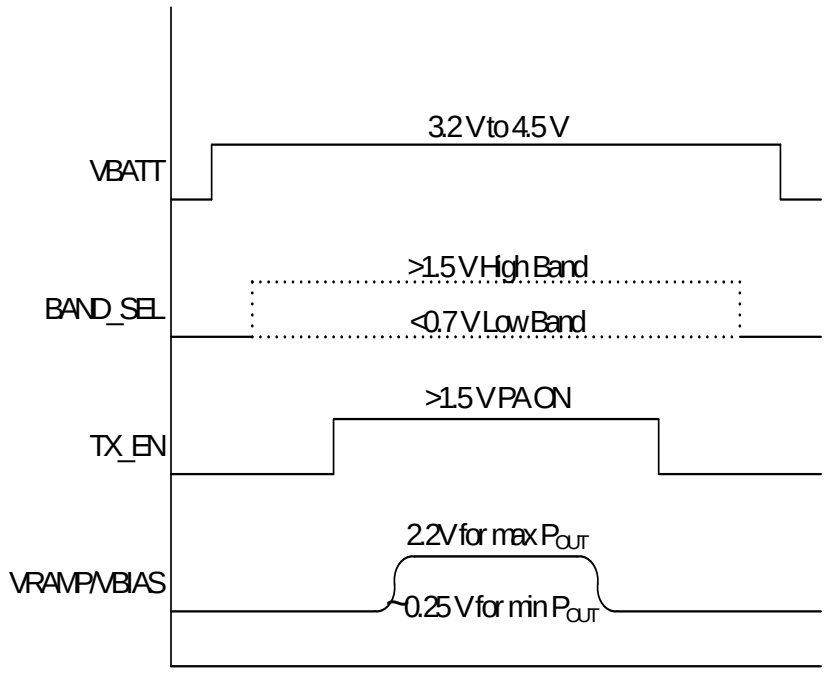
- Transient Spectrum

Switching transients occur when the up and down power ramps are not smooth enough, or suddenly change shape. If the control slope of a PA has an inflection point within the output power control range, or if the slope is too steep, switching transients will result. In RF3183 all stages are kept constantly biased and the output power is controlled by changing the collector voltage according to Equation 1. Inflection points are eliminated by this design. In addition, the steepness of the power control slope is reduced because V_{RAMP} actively controls output power over a larger voltage range than many other power amplifiers.

- Harmonics

Harmonics are natural products of high efficiency, saturated power amplifiers. An ideal, class 'E', saturated power amplifier will produce a perfect square wave. Looking at the Fourier transform of a square wave reveals high harmonic content. Although this is common to all saturated power amplifiers, there are other factors that contribute to harmonic content as well. With many power control methods, a peak power detector is used to rectify and sense forward power. Through the rectification process, there is additional squaring of the waveform resulting in higher harmonics. The RF3183 has no need for the detector diode; therefore, the harmonics coming out of the PA should represent maximum power of the harmonics throughout the transmit chain. This is based on proper harmonic termination of the transmit port. The receive port termination on antenna switch as well as the harmonic impedance from the switch itself will have an impact on harmonics. These terminations should be adjusted to correct problems with harmonics.

GMSK Power On/Off Sequence



Power On Sequence:

1. Apply VBATT
2. Apply BAND_SEL
3. Apply RFIN
4. Apply minimum VRAMP/VBIAS (~0.25V)
5. Apply TX_EN
6. Ramp VRAMP for desired output power

The Power Down Sequence is the reverse order of the Power On Sequence.

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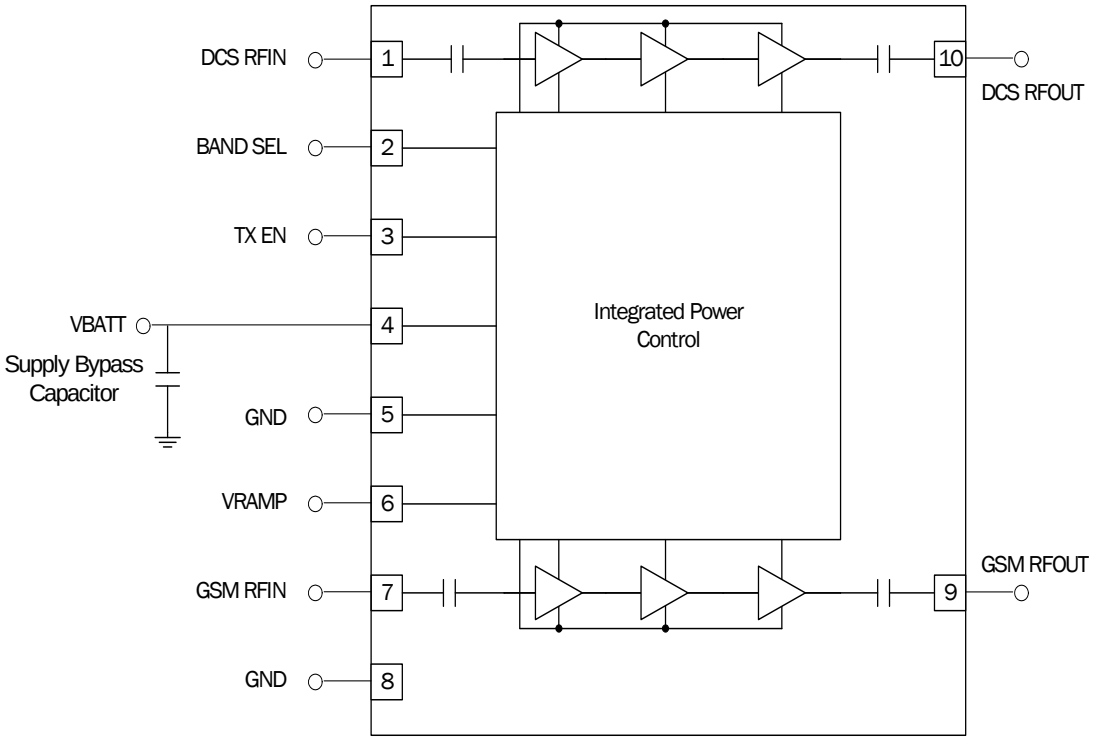
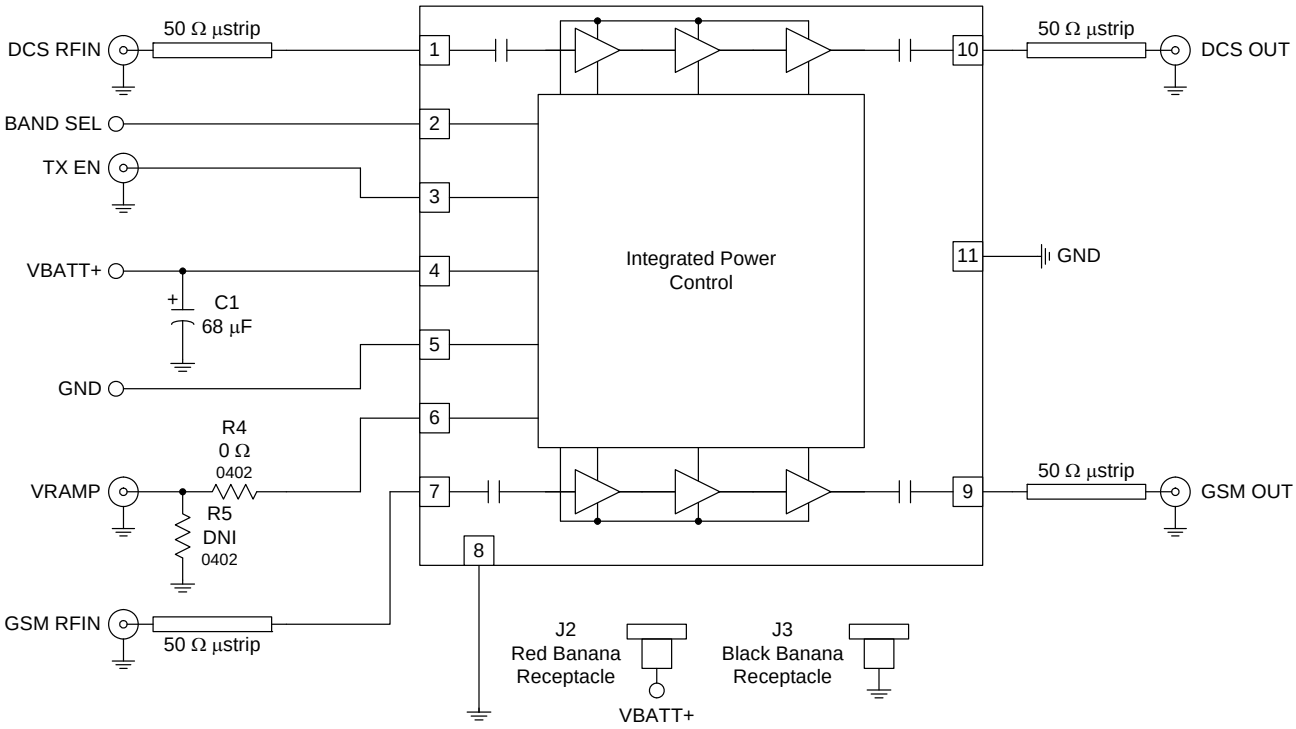
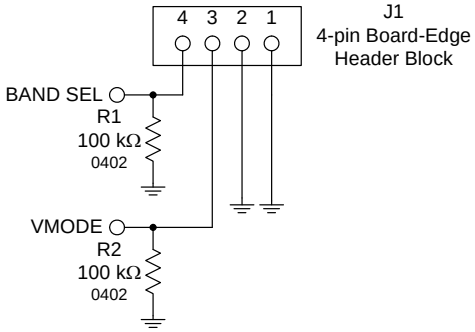
Application Schematic



Evaluation Board Schematic





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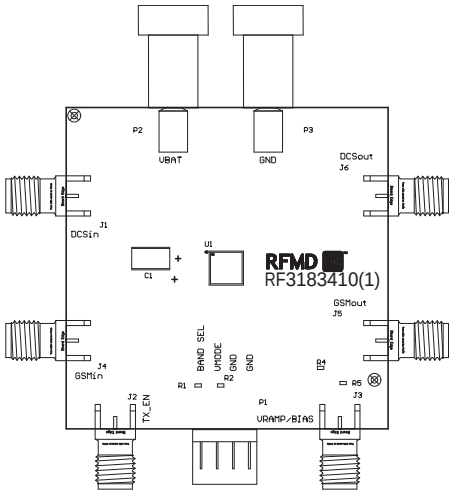
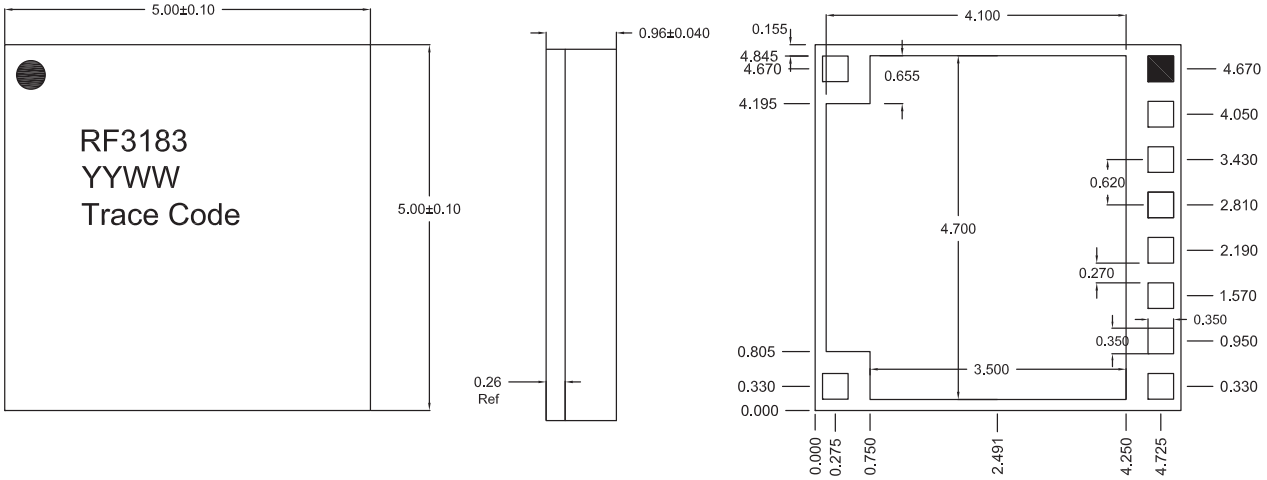
Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.046”, Board Material Rogers RO4003, Multi-Layer



Package Drawing



NOTES:
1. SHADED AREAS REPRESENT PIN 1 LOCATION.
2. FILL IN THE YYWW NOTATION WITH THE DATE CODE
   YY = YEAR
   WW = WORK WEEK
   TRACE CODE TO BE ASSIGNED BY SUBCON

PCB Design Requirements

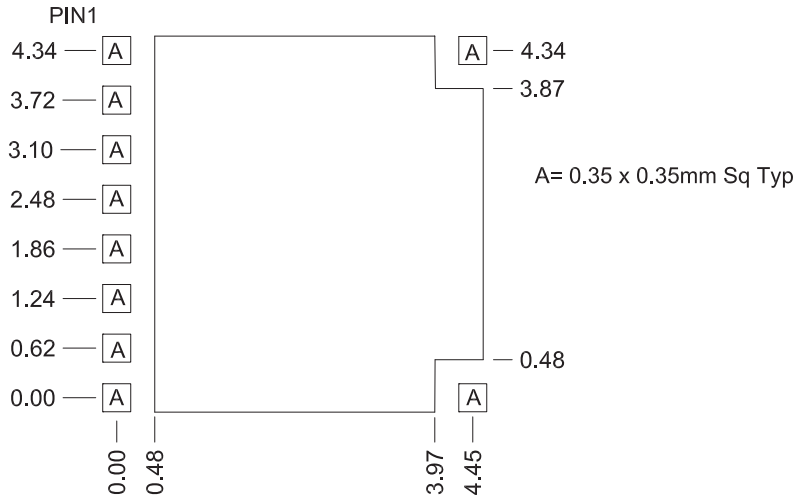
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

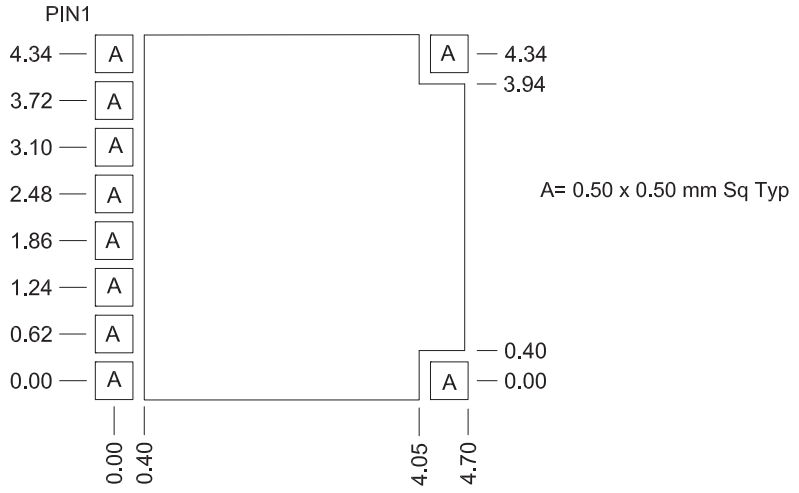
PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



METAL LAND PATTERN



SOLDER MASK PATTERN

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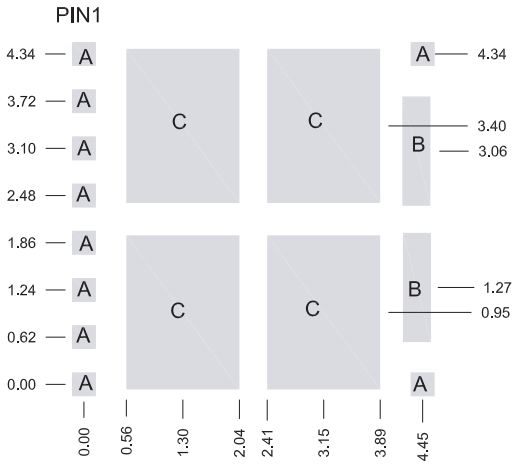
PCB Stencil



A= 0.31 mm Sq Typ
B= 0.37 x 1.44 mm Typ
C= 1.48 x 2.02 mm Typ

Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF3183TR13	13 (330)	4 (102)	12	8	Single	2500

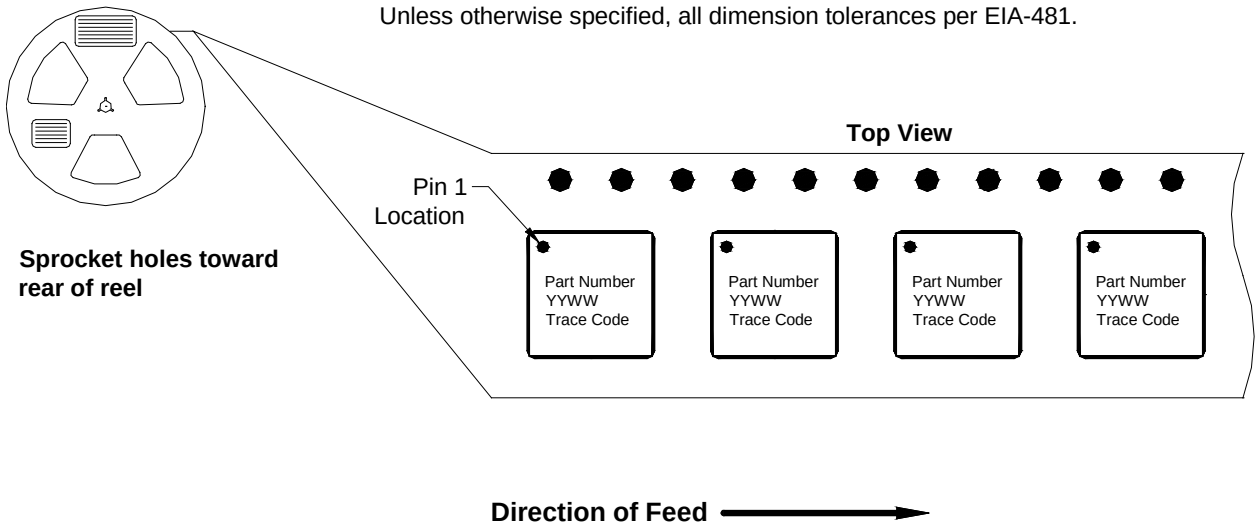


Figure 1. 5mmx5mm (Carrier Tape Drawing with Part Orientation)

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