CV210-203A

410 – 485 MHz Dual-Branch Downconverter

The Communications Edge ™

Product Information

Product Features

- High dynamic range downconverter with integrated LO and IF amplifiers
- Dual channels for diversity
- Up to +28.5 dBm Input IP3
- +12 dBm Input P1dB
- RF: 410 – 485 MHz
- IF: 46 MHz
- +5V Single supply operation
- Pb-free 6mm 28-pin QFN package
- High-side LO configuration
- Common footprint with other PCS/UMTS/cellular versions

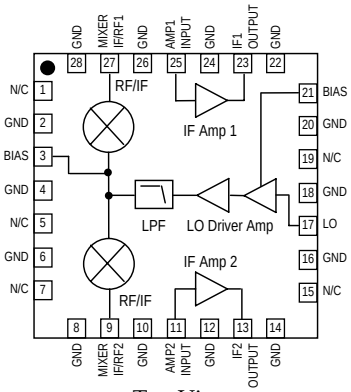
Product Description

The CV210-203A is a dual-channel high-linearity downconverter designed to meet the demanding performance, functionality, and cost goals of current and next generation mobile infrastructure basestations. It provides high dynamic range performance in a low profile lead-free/RoHS-compliant surface-mount leadless package that measures 6 x 6 mm square.

It is ideally suited for high dynamic range receiver front ends using diversity receive channels. Functionality includes frequency conversion and IF amplification, while an integrated LO driver amplifier powers the passive mixer. The MCM is implemented with reliable and mature GaAs MESFET and InGaP HBT technology.

Typical applications include frequency downconversion used in mobile base transceiver stations.

Functional Diagram



Top View

Specifications (1)

Parameters	Units	Min	Typ	Max	Comments
RF Frequency Range	MHz		410 – 485		
LO Frequency Range	MHz		456 – 531		
IF Center Frequency Range	MHz		46		See note 2
SSB Conversion Gain	dB		10.5		Temp = 25 °C
Gain Drift over Temp (-40 to 85° C)	dB	-1.5	±0.5	1.5	Referenced to +25 °C
Input IP3	dBm		+23		RF = 410 – 420 MHz, See note 3
Input IP3	dBm		+27.5		RF = 450 – 460 MHz, See note 3
Input IP3	dBm		+28.5		RF = 475 – 485 MHz, See note 3
Input IP2	dBm		+42.5		
Input 1 dB Compression Point	dBm		+10.5		
Noise Figure	dB		11		See note 4
LO Input Drive Level	dBm	-2.5	0	+2.5	
LO-RF Isolation	dB		25		P_{LO} = 0 dBm
LO-IF Isolation	dB		35		P_{LO} = 0 dBm
Branch-Branch Isolation	dB		65		
Return Loss: RF Port	dB		25		
Return Loss: LO Port	dB		12		
Return Loss: IF Port	dB		22		
Operating Supply Voltage	V	+4.9	+5	+5.1	
Supply Current	mA	320	390	475	
Thermal Resistance	°C / W			27	
Junction Temperature	°C			160	See note 5

1. Specifications when using the application specific circuit (shown on page 3) with a high-side LO = 0 dBm in a downconverting application at 25° C.
2. IF matching components affect the center IF frequency. Proper component values for other IF center frequencies than shown can be provided by emailing to applications.engineering@wj.com.
3. Assumes the supply voltage = +5 V. IIP3 is measured with Δf = 1 MHz with RF_{in} = -5 dBm / tone.
4. Assumes LO injection noise is filtered at the thermal noise floor, -174 dBm/Hz, at the RF, IF, and Image frequencies.
5. The maximum junction temperature ensures a minimum MTTF rating of 1 million hours of usage.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +150 °C
RF Port Input Power (pins 9, 27) Maximum RF Port Input Power is for +25 dBm for 1 hour cumulative over 10 years lifetime.	+25 dBm
DC Voltage	+5.5 V
Junction Temperature	+220 °C

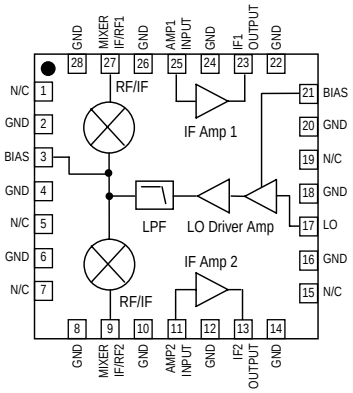
Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

Part No.	Description
CV210-203AF	410 – 485 MHz Dual-Branch Downconverter (lead-free/RoHS-compliant 6x6mm QFN package)

Specifications and information are subject to change without notice

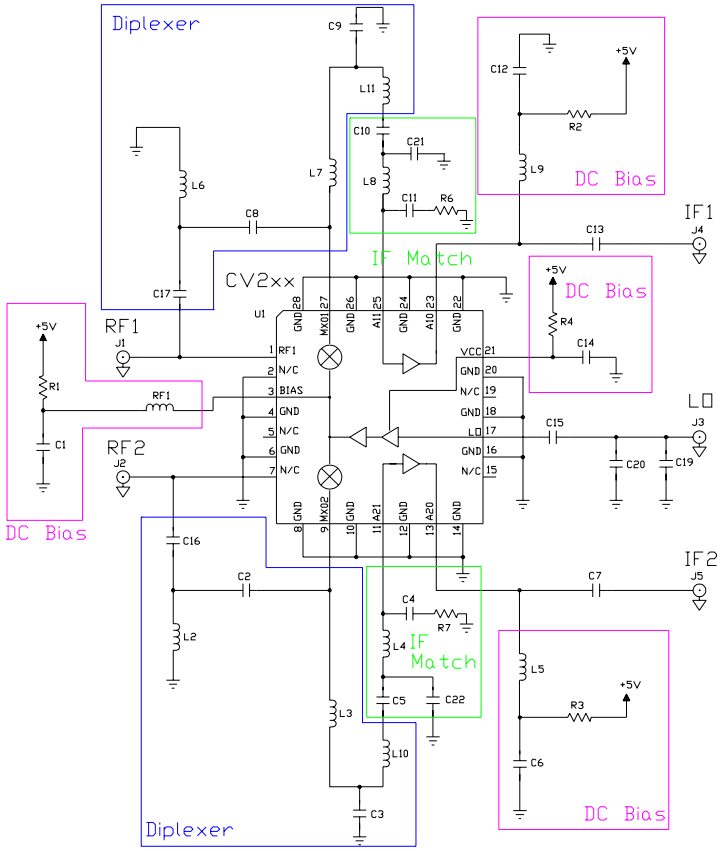
Device Architecture / Application Circuit Information



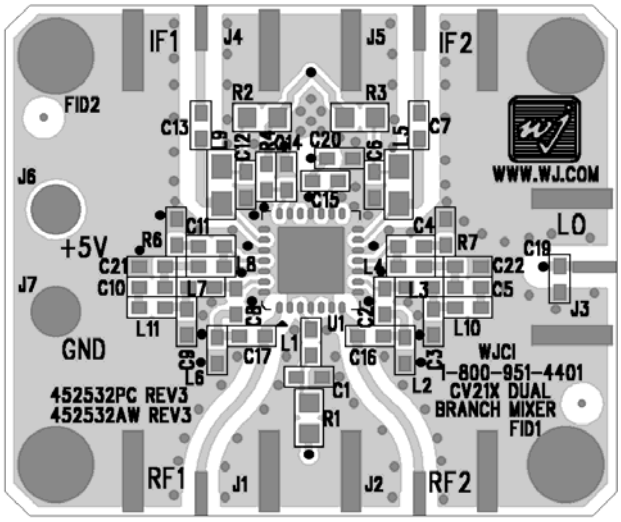
Typical Downconverter Performance Chain Analysis (Each Branch)

Stage	Gain (dB)	Input P1dB (dBm)	Input IP3 (dBm)	NF (dB)	Current (mA)	Cumulative Performance			
						Gain (dB)	Input P1dB (dBm)	Input IP3 (dBm)	NF (dB)
LO Amp / MMIC Mixer	-9	11	25	9.3	60	-9	11	25	9.3
IF Amplifier	19	2	22	1.8	150	10	8	24	11
CV210-203A	**Cumulative Performance**				**360***	**10**	**+8**	**+24**	**11**

* The 2nd branch includes another mixer and IF amplifier, which increases the total current consumption of the MCM to be 360 mA.



Printed Circuit Board Material:
.014" FR-4, 4 layers, .062" total thickness



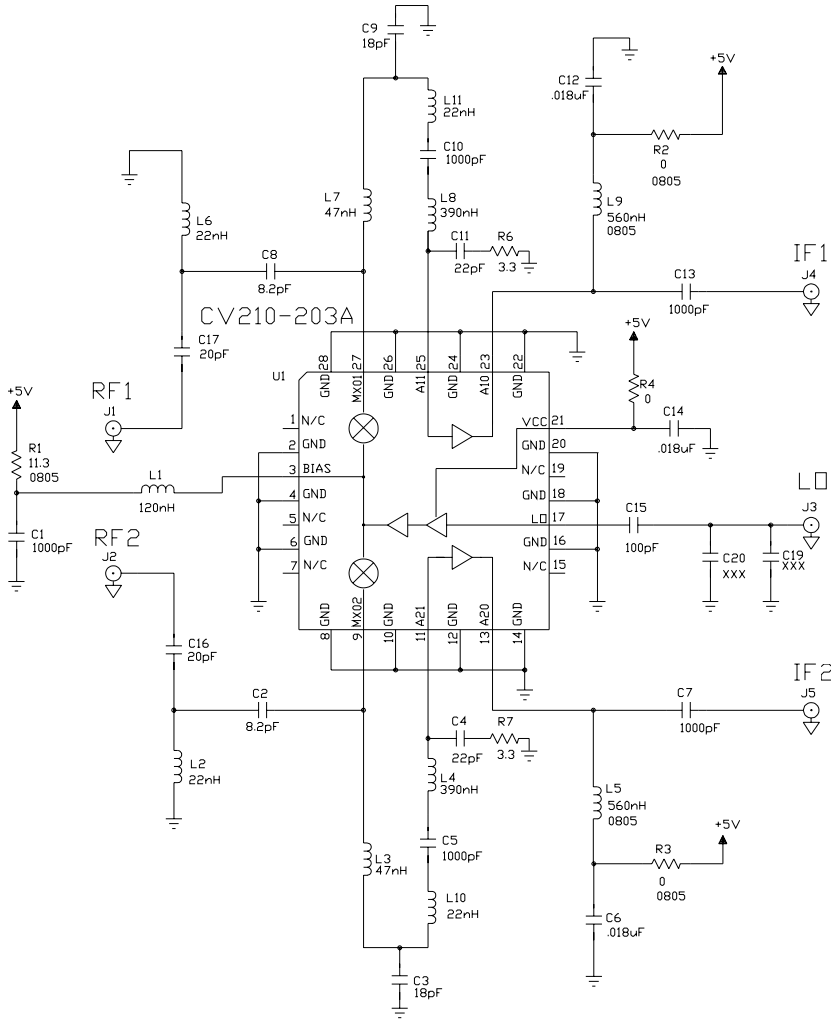
CV210-203A: The application circuit can be broken up into three main functions as denoted in the colored dotted areas above: RF/IF diplexing (blue), IF amplifier matching (green), and dc biasing (purple). There are various placeholders for chip components in the circuit schematic so that a common PCB can be used for all WJ dual-branch converters. Further details are given in the Application Note located on the website titled "CV2xx Series - PWB Design Guidelines".

External Diplexer: In a downconversion application, the incoming RF signal impinges on the switching elements of the mixer; the interaction with these switches produces a signal at the IF frequency. The two signals (RF and IF) are directed to the appropriate ports by the external diplexer. A six-element diplexer is used in the circuit implementation.

IF Amplifier Matching: The IF amplifier requires matching elements to optimize the performance of the amplifier to the desired IF center frequency. Since IF bandwidths are typically on the order of 5 to 10%, a simple two element matching network, in the form of either a high-pass or low-pass filter structure, is sufficient to match the MMIC IF amplifier over these narrow bandwidths. Proper component values for other IF center frequencies can be provided by emailing to applications.engineering@wj.com.

DC biasing: DC bias must be provided for the LO and IF amplifiers in the converter. R1 sets the operating current for the last stage of the LO amplifier and is chosen to optimize the mixer LO drive level. Proper RF chokes and bypass capacitors are chosen for proper amplifier biasing at the intended frequency of operation. The "+5 V" dc bias should be supplied directly from a voltage regulator.

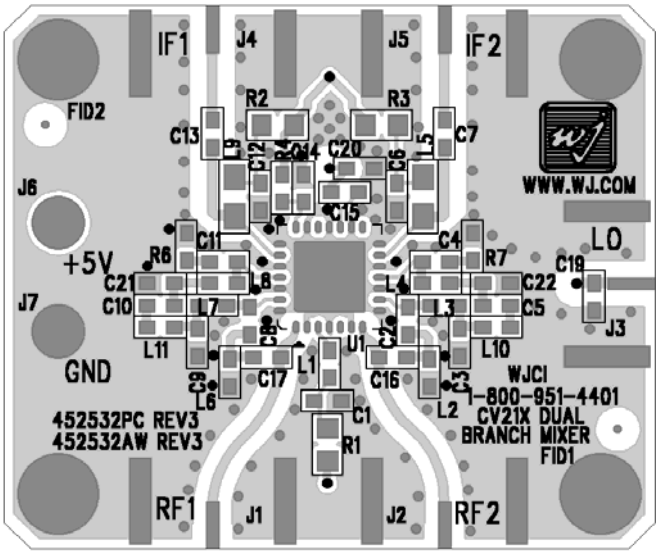
Application Circuit: IF = 46 MHz



Bill of Materials

Ref. Desig.	Component	Size
R1	11.3 Ω chip resistor	0805
R2, R3, R4	0 Ω chip resistor	0603
R6, R7	3.3 Ω chip resistor	0603
C1, C5, C10, C15	1000 pF chip capacitor	0603
C2, C8	8.2 pF chip capacitor	0603
C3, C9	18 pF chip capacitor	0603
C4, C11	22 pF chip capacitor	0603
C6, C12, C14	.018 µF chip capacitor	0603
C7, C13	100 pF chip capacitor	0603
C16, C17	20 pF chip capacitor	0603
L1	120 nH chip inductor	0603
L2, L6	22 nH chip inductor	0603
L3, L7	47 nH chip inductor	0603
L4, L8	390 nH chip inductor	0603
L5, L9	560 nH chip inductor	0805
L10, L11	22 nH chip inductor	0603
C19, C20, C21, C22	Do Not Place	
U1	CV210-203A WJ Converter	QFN

PCB Layout

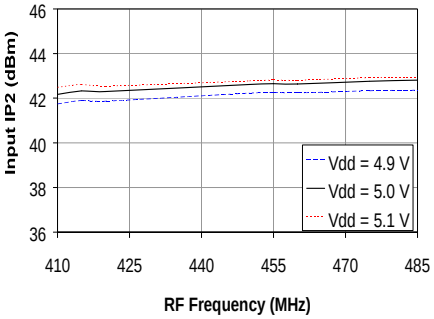


Circuit Board Material: .014” FR-4, 4 layers, .062” total thickness

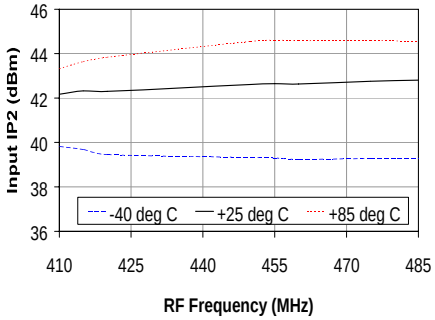
Specifications and information are subject to change without notice

CV210-203APCB46 Application Circuit Performance Plots

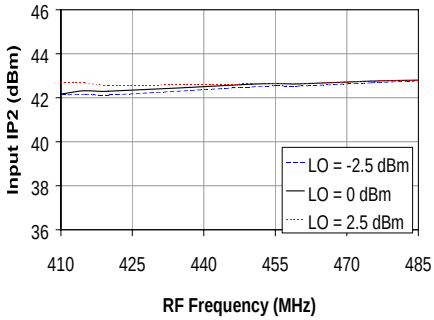
Input IP2 vs RF Frequency over Vdd
25 deg C, LO = 0 dBm, IF = 46 MHz, high-side LO



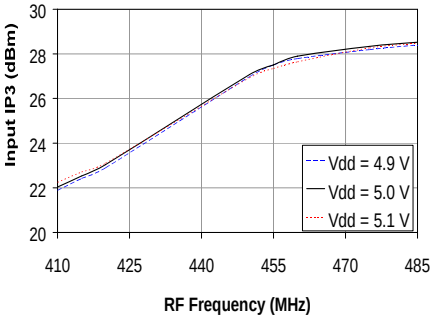
Input IP2 vs RF Frequency over Temp
LO = 0 dBm, IF = 46 MHz, high-side LO



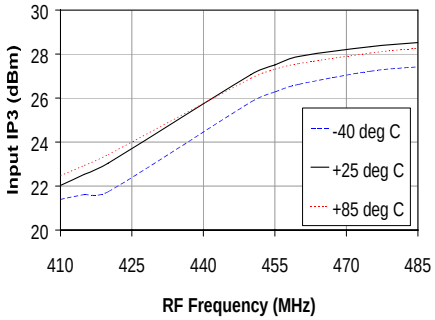
Input IP2 vs RF Frequency over LO Power
25 deg C, IF = 46 MHz, high-side LO



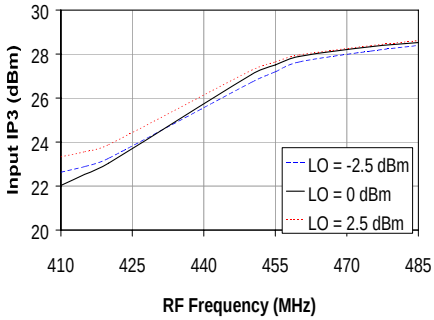
Input IP3 vs RF Frequency over Vdd
25 deg C, LO = 0 dBm, IF = 46 MHz, high-side LO



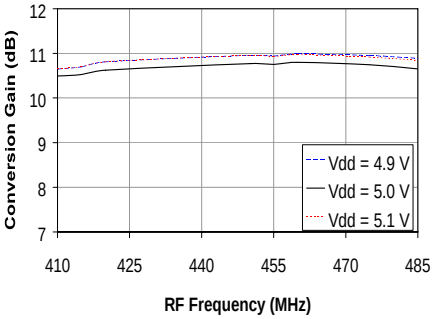
Input IP3 vs RF Frequency over Temp
LO = 0 dBm, IF = 46 MHz, high-side LO



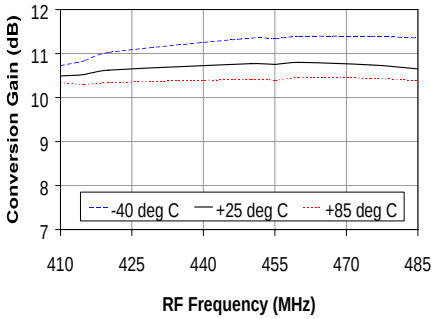
Input IP3 vs RF Frequency over LO Power
25 deg C, IF = 46 MHz, high-side LO



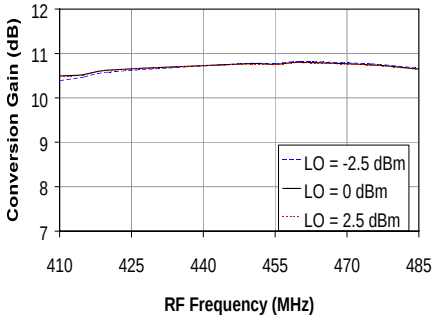
Conversion Gain vs RF Frequency over Vdd
25 deg C, LO = 0 dBm, IF = 46 MHz, high-side LO



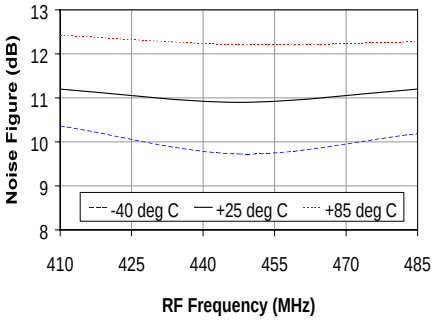
Conversion Gain vs RF Frequency over Temp
LO = 0 dBm, IF = 46 MHz, high-side LO



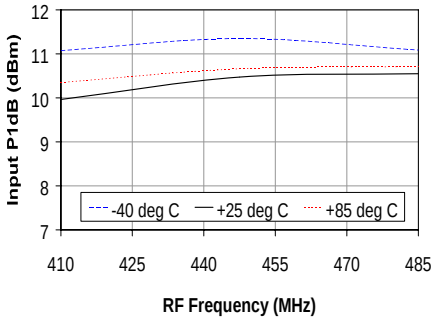
Conversion Gain vs RF Frequency over LO Power
25 deg C, IF = 46 MHz, high-side LO



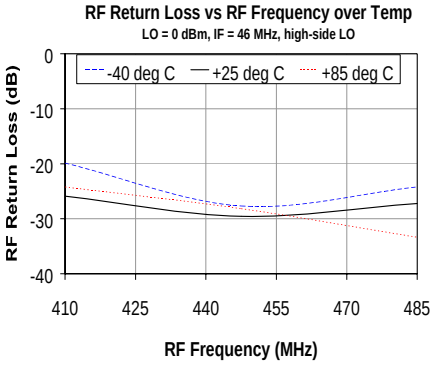
Noise Figure vs RF Frequency over Temp
LO = 0 dBm, IF = 46 MHz, high-side LO

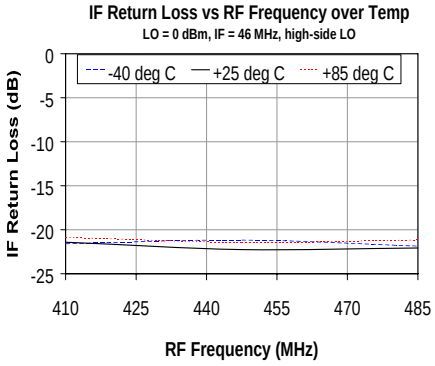


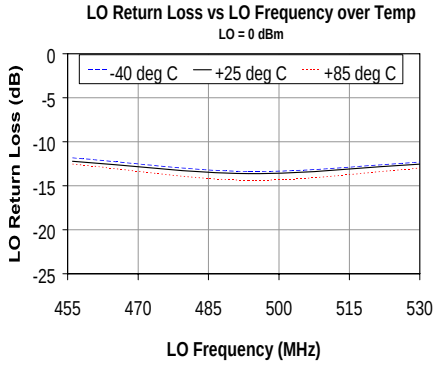
Input P1dB vs RF Frequency over Temp
LO = 0 dBm, IF = 46 MHz, high-side LO

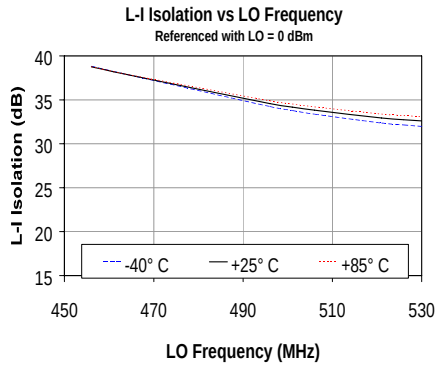


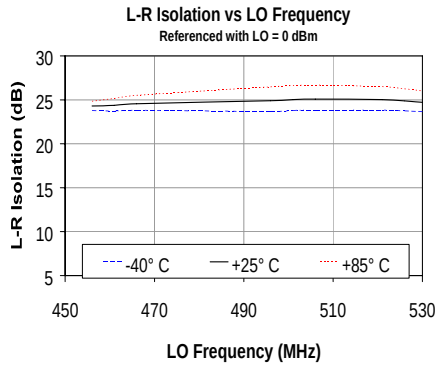
CV210-203APCB46 Application Circuit Performance Plots (cont'd)

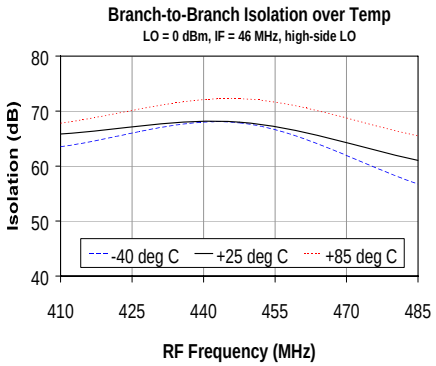








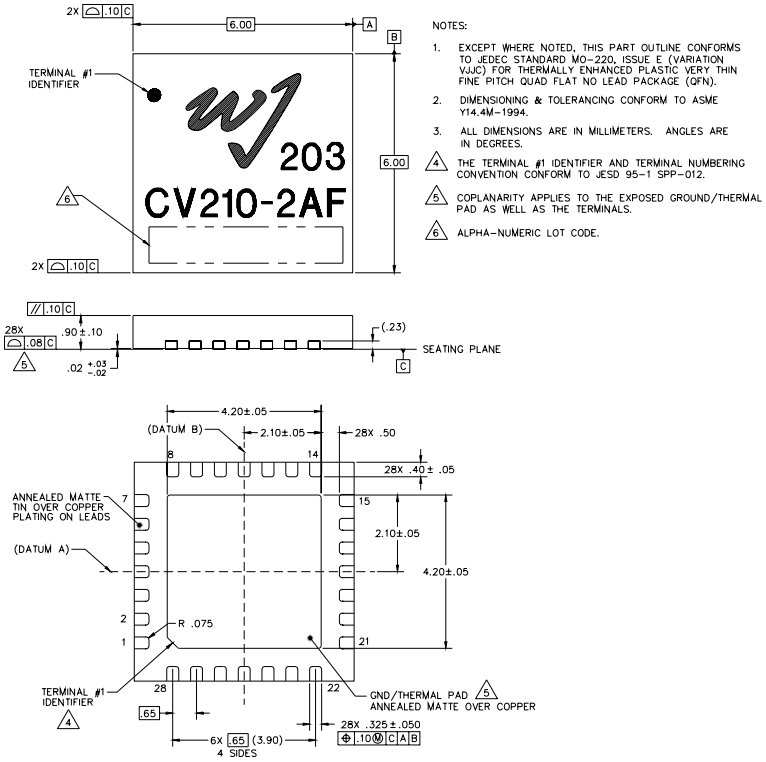




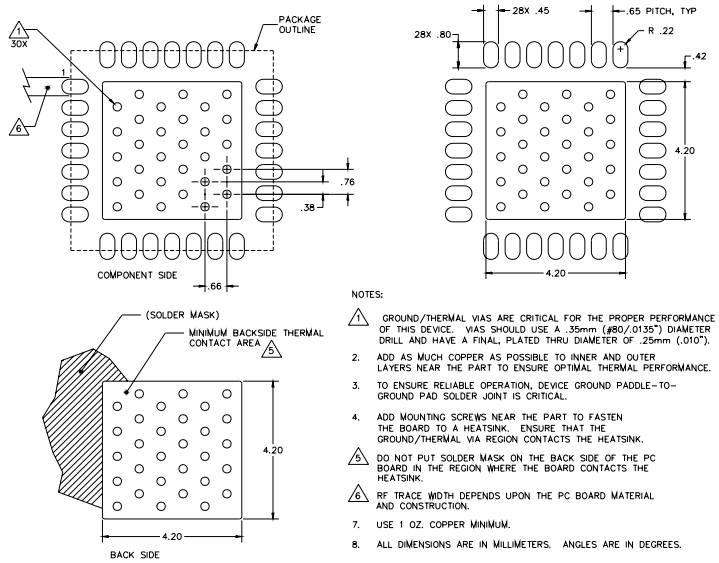
CV210-203AF Mechanical Information

This package is lead-free/RoHS-compliant. It is compatible with both lead-free (maximum 260°C reflow temperature) and leaded (maximum 245°C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

Outline Drawing



Mounting Configuration / Land Pattern



Product Marking

The component will be lasermarked with a "CV210-2AF" product label with a four-digit alphanumeric lot code on the top surface of the package. A "203" lasermark will be shown above the "CV210-2AF" to differentiate this product with the CV210-2AF.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ≥ 500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class III
Value: Passes ≥ 500V to <1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 2 at +260°C convection reflow
Standard: JEDEC Standard J-STD-020

Functional Pin Layout

Pin	Function	Pin	Function
1	No Connect	15	No Connect
2	GND	16	GND
3	LO Amp Bias	17	LO input
4	GND	18	GND
5	No Connect	19	No Connect
6	GND	20	GND
7	No Connect	21	+5 V
8	GND	22	GND
9	Ch. 2 Mixer RF Input / IF Output	23	Channel 1 IF Amp Output / Bias
10	GND	24	GND
11	Channel 2 IF Amp Input	25	Channel 1 IF Amp Input
12	GND	26	GND
13	Channel 2 IF Amp Output / Bias	27	Channel 1 Mixer RF Input / IF Output
14	GND	28	GND