MAAP-011106

Power Amplifier, 71 - 86 GHz

Rev. V2

Features

- 4 Stage Power Amplifier for E Band
- 20 dB Gain
- 15 dB input and output match
- 25 dBm saturated output power
- 30 dBm OIP3
- Variable gain with adjustable bias
- Integrated detector
- Bare die
- RoHS* compliant and 260°C reflow compatible
- HBM ESD rating of 100 V
- Size: 3780 x 2500 x 50 µm

Description

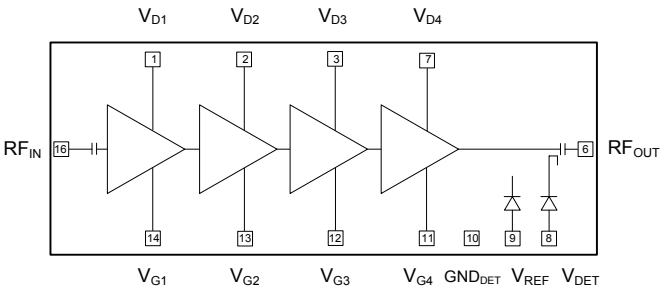
The MAAP-011106 is a bare die power amplifier that operates from 71 - 86 GHz. The amplifier provides 20 dB small signal gain. The input and output are matched to 50 Ω with bond wires to external board. It is designed for use as a power amplifier stage in transmit chains and is ideally suited for E band point to point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

Ordering Information

Part Number	Package
MAAP-011106-DIE	Die in vacuum release gel pack

Chip Device Layout



Pad Configuration

Pad No.	Function	Pad No.	Function
1	V_D1	9	V_{REF}
2	V_D2	10	GND_{DET}
3	V_D3	11	V_G4
4	V_D4	12	V_G3
5	GND	13	V_G2
6	RF_{OUT}	14	V_G1
7	GND	15	GND
8	V_{DET}	16	RF_{IN}
		17	GND

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Power Amplifier, 71 - 86 GHz

Electrical Specifications[1]: Freq. = 71 - 86 GHz, V_D = 4 V, I_D = 720 mA, T_A = 25°C

Parameter	Units	Min.[2]	Typ.	Max.
Gain	dB	18	20	-
Input Return Loss	dB	-	15	-
Output Return Loss	dB	-	15	-
P1dB	dB	-	23	-
P_{OUT} with P_{IN} = 13 dBm	dBm	-	25	-
P_{SAT} (P4dB)	dBm	24	25	-
OIP3 (worst tone)	dBm	-	30	-
IIP3 (worst tone) for Gain = 20 turned down to -5 dB	dBm	-	10	-

1. Quiescent DC Bias: I_D1= 60 mA, I_D2 = 120 mA, I_D3 = 240 mA, I_D4 = 300 mA. Total DC power = 2.88 W
2. Minimum limits are the on-wafer minimum test limits

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Drain Voltage	+4.3 V
Drain Current	935 mA
Gate Bias Voltage (V_G1,2,3,4)	-1.5 V < V_G < 0 V
Input Power	+16 dBm
Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C
Junction Temperature[5]	+150°C
Thermal Resistance	16.15°C/W

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.

Handling Procedures

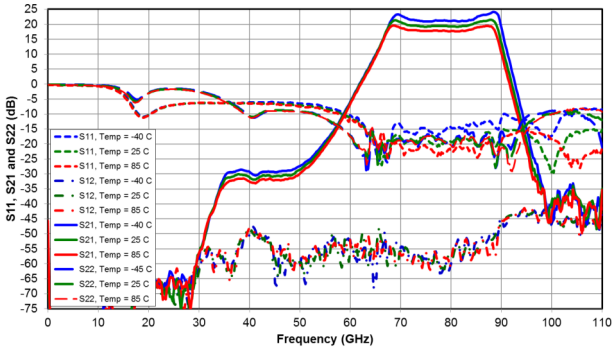
Please observe the following precautions to avoid damage:

Static Sensitivity

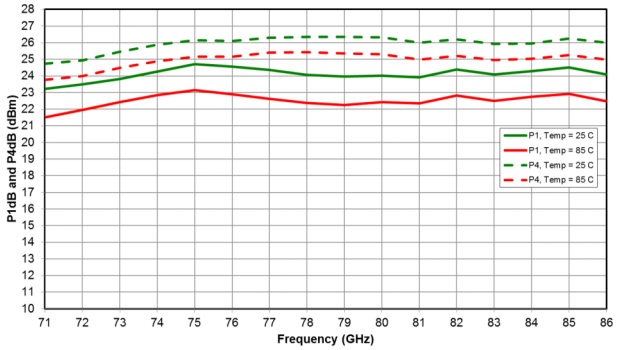
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these static sensitive devices.

Typical Performance Curves

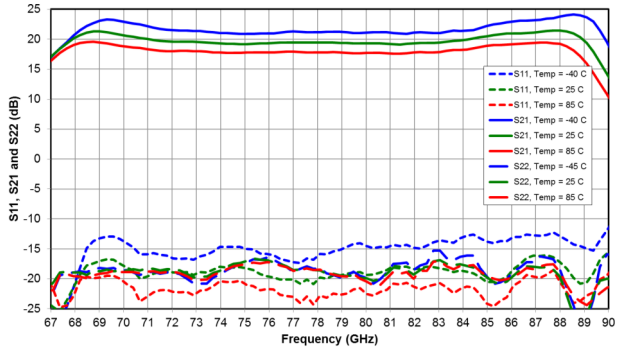
S-Parameters (Wideband)



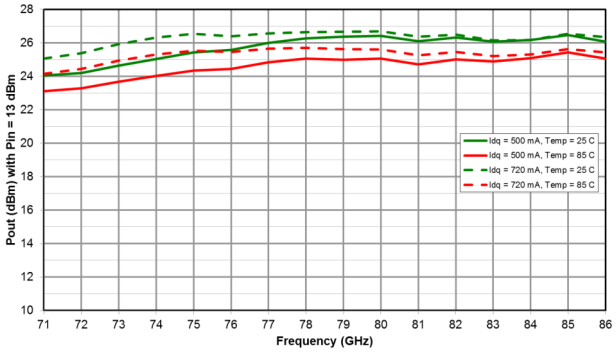
P1dB and P4dB



S-Parameters

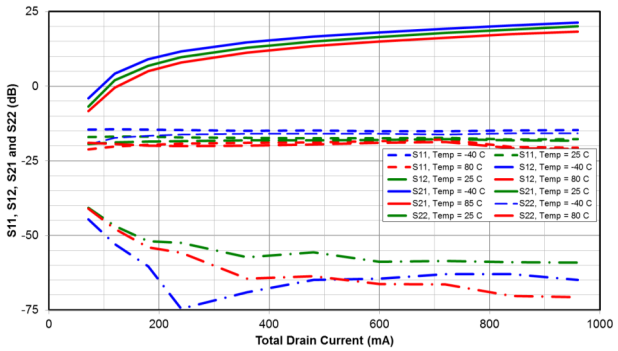


P_{OUT} @ P_{IN} = 13 dBm

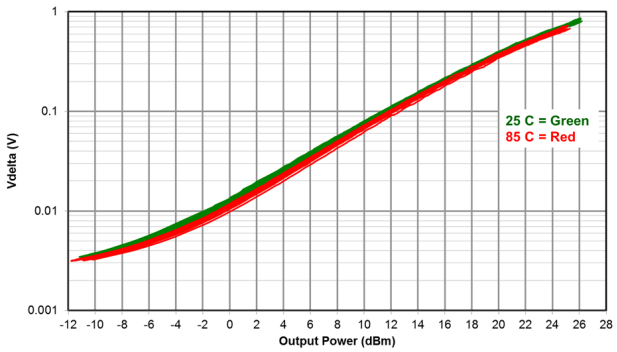


Typical Performance Curves

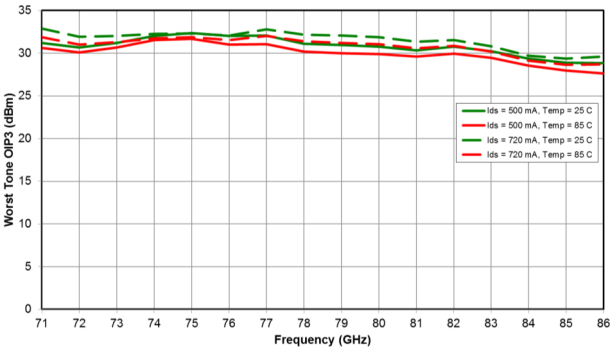
S-Parameters @ 80 GHz vs. Current



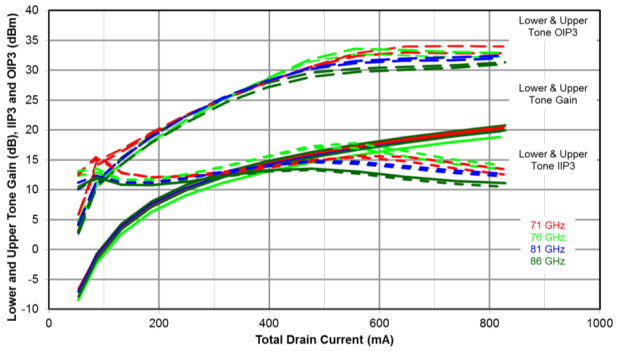
Detector Delta Voltage vs. Output Power



Worst Tone Output IP3

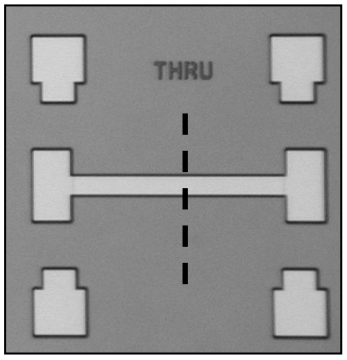


Lower and Upper Tone Gain, IIP3 and OIP3 vs. Current



Calibration Plane

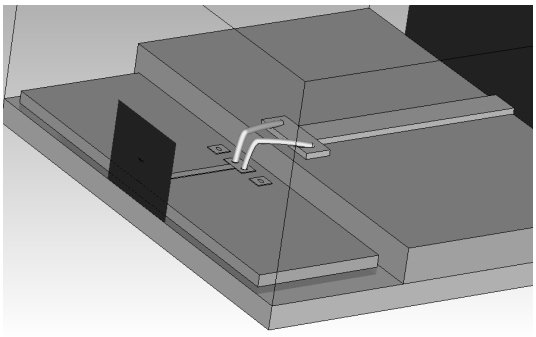
All data was measured on die with 200 µm pitch probes. The calibration plane is at the middle of the through, 178.5 µm from the middle of the RF pad.

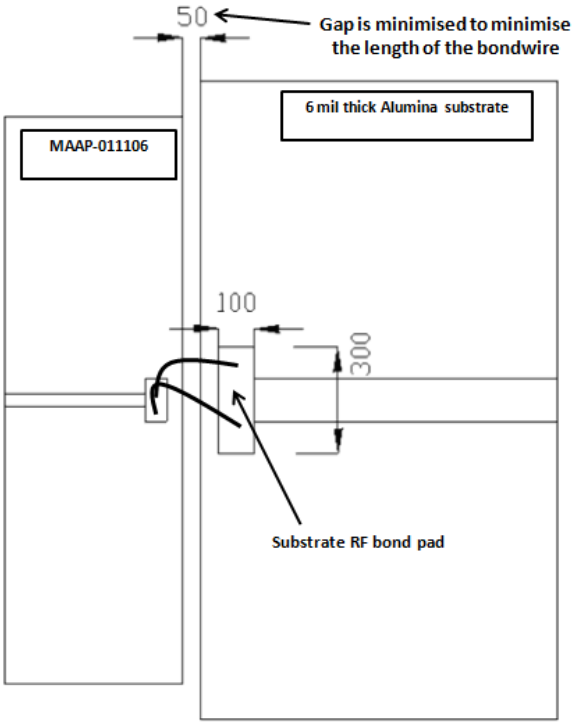


App Note [1] Biasing -
All gates should be pinched-off (V_G < -1 V) before applying drain voltage (V_D = 4 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is V_D = 4 V, I_D1 = 60 mA, I_D2 = 120 mA, I_D3 = 240 mA and I_D4 = 300 mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

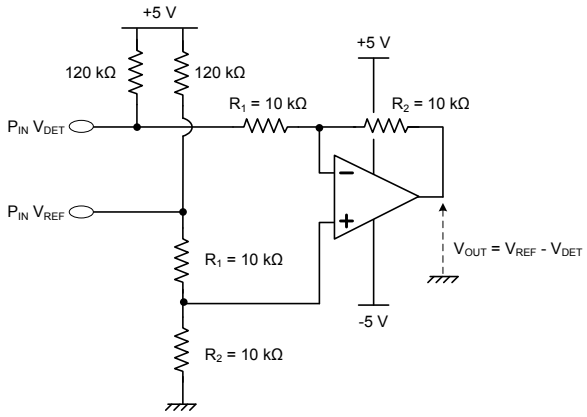
App Note [2] Bias Arrangement -
Each DC pin (V_D1,2,3,4 and V_G1,2,3,4) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.

App Note [3] Wire Bonding -
The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 25 µm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below.

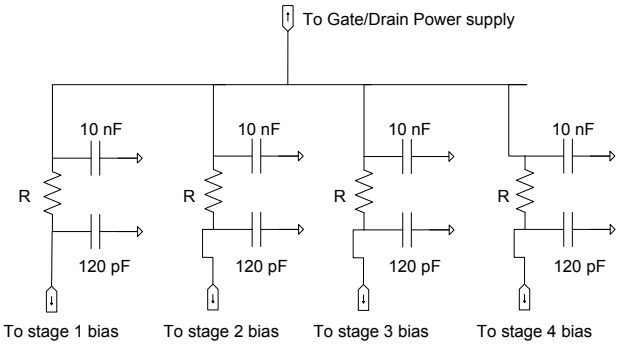




App Note [4] Detector biasing schematic -
As shown in the schematic below, the power detector is biased by matched 120 kΩ resistors to a +5 V supply. The difference voltage between V_{DET} and V_{REF} pins can be obtained using the op-amp differencing circuit shown below.



App Note [5] Common Gates and Drains -
When biasing the device with only a single gate or drain source additional isolation is required between each stage. On the gate side a 10 Ω resistor should be placed in series and tied together in a star to a common supply. The drain side resistance should be reduced to less than 5 Ω to minimize any voltage drop across the resistor. Suitable bias pass capacitance should still be applied to each stage as per App Note [2].



Layout Dimensions